UNIVERSITÀ DEGLI STUDI DI NAPOLI
"FEDERICO II"

Scuola Politecnica e delle Scienze di Base

Area Didattica di Scienze Matematiche Fisiche e Naturali

Dipartimento di Fisica "Ettore Pancini"

Laurea Magistrale in Fisica

Automatic Generation of Redundant Configuration in SRAM-based FPGAs for Hadron Fluence Sensors

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Anno Accademico 2021/2022

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Introduction

Digital electronics is very important for real-time data processing, so it is necessary in physics experiments and, in particular, in high energy physics experiments. Furthermore, it finds more and more application fields and in many of these it is necessary to cope with or to operate in the presence of radiation (e.g. energy, aerospace, medical, and others). Radiation effects depend on the impacting particles energy and type.

As discuss above, it is important to develop sensors to measure the radiation in the environment.

The radiation effects can be summarized in two categories: single event effects (SEE) and total dose effects (TDE). The SEEs can be divided into two subcategories, soft and hard errors, depending on whether they can be eliminated by power cycling the device or they cause a permanent damage to it. The SEUs are particular soft errors that may happen in memory cells, including latches or registers of central processing units (CPUs) and field-programmable gate arrays (FPGAs).

Static random access memorie (SRAM) cells are used to measure high-energy hadrons. To read SRAMs, it is necessary to use an external component, such as an FPGA or CPU and SRAM to read the upsets.

The PHI experiment, funded by INFN Commissione Scientifica Nazionale V in 2021-2022, proposes to use SRAM-based FPGAs to realize high-energy hadron fluence sensors in a single device. The proposed sensors use a redundant con-

figuration, to self-determine the upsets in memory without the aid of external memories.

The core of my thesis work was the development and testing of a software tool to automate and optimize the generation of the above-mentioned redundancy.

This thesis is organized as follows.

In chapter 1, I will introduce the effects of radiation in electronic components, with particular attention to single event effects in SRAMs.

In chapter 2, I will talk of instruments that sense and measure radiation emissions or levels of radiation and will focus on hadron fluence sensors.

In chapter 3, I will discuss single event effects (SEE) on SRAM-based FPGAs and the solutions to mitigate single event upset (SEU) effects on FPGAs configuration memory.

Finally, in chapter 4, I will present my automatic methodology to generate a redundant configuration for SRAM-based FPGAs and describe test results.

Chapter 1

Radiation Damage in Electronic Components

Digital electronics finds more and more application fields and in many of these it is necessary to cope with (or to operate in presence of) radiation (e.g. medical, energy, aerospace, and others). In the following, we will show which kind of effects are brought by radiation in several electronic components and in detail how technology advancements worsen or mitigate these effects. It is also important to clarify immediately that different types of devices are affected differently. As far as it concerns this thesis we focus on silicon-based programmable digital devices, specifically Field Programmable Gate Arrays (FPGAs), which we will introduce in next chapter.

1.1 Radiation environments

Radiation is the transfer of energy by means of particles (including photons). It is possible to find radiation effects in a huge number of environments: space, terrestrial or artificial ones.

For each environment there are different specter of particles, so it is very important devices must be designed to operate in assigned environment.

In Table 1.1 we can see in schematic way, the different type of particles which type of interactions there are. This table shows how the various particles cause ionization or displacement damage phenomenas primary or secondary effects, some particles (e.g. protons) can cause different effects depending on the energy. In the same table the types of interaction of other particles are highlighted.

Radiation type	Energy range	Type of interaction	Primary effects	Secondary effects
Photons	< 0.1 MeV	Photoelectric effect	Ionizing phenomena	Displacement damage
	0.3 – 3 MeV	Compton effect		
	< 0.024 MeV	Pair production		
Neutrons	> 0.025 eV	Show diffusion, capture by nuclei	Displacement damage	Ionizing phenomena
	< 10 MeV	Elastic scattering, capture nuclear excitation		
	> 10 MeV	Elastic scattering, inelastic scattering, various nuclear reactions, secondary charged reaction products		
Electrons	< 10 MeV	Collision, Coulomb attraction	Ionizing phenomena	
	> 10 MeV	Bremsstrahlung		
Protons	< 50 MeV	Coulomb attraction elastic scattering	Ionizing phenomena	
	> 50 MeV	Inelastic scattering	Displacement damage	Ionizing phenomena

Table 1.1: Types of particle interaction.

1.1.1 Space radiation

Radiation in space consists in three components: a) particles trapped in the Earth's magnetic field; b) particles shot into space during solar flares (solar particle events); c) galactic cosmic rays, which are mostly high-energy protons and heavy ions from outside our solar system. All these types are ionizing radiation and depend on two causes: flares and coronal mass ejections (high-energy proton emitted by the sun), or galactic cosmic rays (high-energy ions of elements that have had all their electrons stripped away) [1]. Table 1.2 lists the maximum energy of

space radiation particles [2] and shows that maximum energy in the environment. As we can see in the table, galactic cosmic rays can have energies of several orders of magnitude higher than other ions.

Particle type	Maximum Energy
Trapped Electrons	10s of MeV
Trapped Protons & Heavy Ions	100s of MeV
Solar Protons	GeV
Solar Heavy Ions	GeV
Galactic Cosmic Ray	TeV

Table 1.2: Maximun energies of particles. Source [2].

1.1.2 Earth atmosphere radiation

Solar radiation travels in the form of electromagnetic waves at the speed of light. The radiation is composed also by other particles generated by cosmic rays, the types of particles generated are: protons, electrons, pions, kaons and neutrinos.

Fig.1.1 shows the calorimeter-like behavior of the atmosphere and how particle showers form from a single incident particle. Usually proton or alfa particles

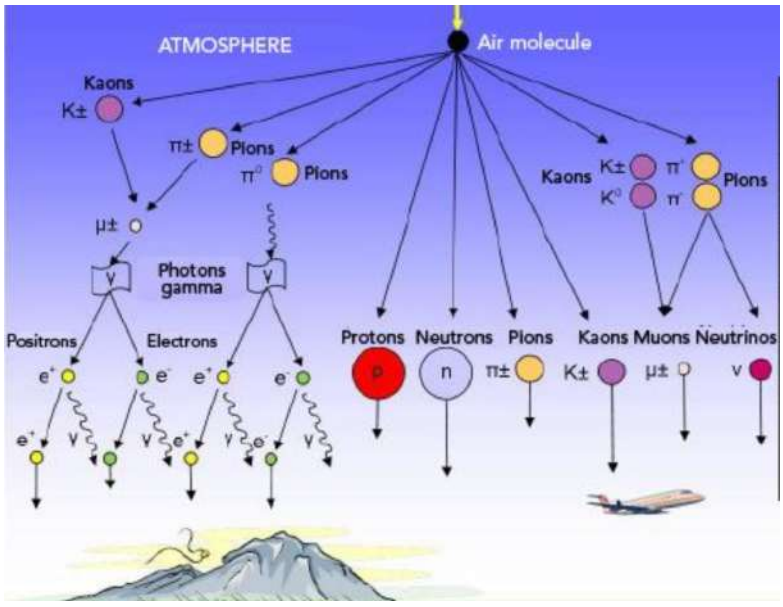

Figure 1.1: Atmospheric radiation.

When cosmic ray radiation hit the atmosphere it can generate particles. At near to 60 km in height this particles are most common, but this particles are still

present in lower zone. Typically at level of the sea they don't represent a problem but they could be in airline fly altitude (10-14 km) (Fig.1.2).

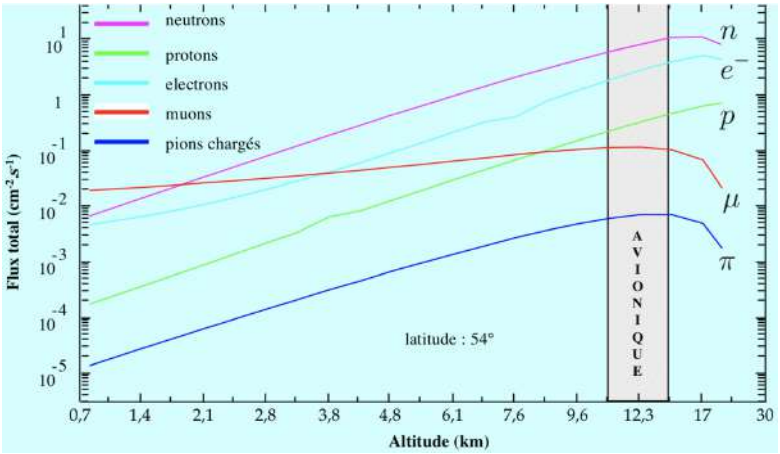

Figure 1.2: Atmospheric radiation for different hight.

1.1.3 Artificial radiation

On the Earth both natural and manmade radiation are present.

Physics experiments can generate radiation especially those of high energy that exploit particle accelerators: KEK (Tsukuba, Japan) where electron-electron collisions are made or CERN (LHC) (Geneva, Switzerland) where proton-proton collisions are made Others manmade sources expose the public to radiation are: medical diagnostic, nuclear power, consumer products, combustible fuels, including gas and coal, televisions, tobacco (polonium-210), smoke detectors, etc.

However, in the last decades radiation became important in new medical treatments, for example with proton-therapy. In Italy there are different structures that allow this type of therapy, i.e. Trento Institute for Fundamental Physics and Applications (TIFPA, Trento) and Laboratori Nazionali del Sud (LNS, Catania), that are proton irradiation facilities.

1.2 Overview of radiation-effects in electronics

Radiation effects depend on the impacting particles energy and type. In any case, these effects can be summarized in two categories: single event effects (SEE) and total dose effects (TDE). Although the origins of these two effects may be similar, the effects could be deeply different. For example, a charged particle can damage the crystal lattice (of the silicon structure) symmetry, in other cases it can deposit charge which causes critical issues. The SEEs can be divided into two sub-categories, soft and hard errors, depending on whether they can be eliminated by power cycling the device or they cause a permanent damage to it. We observe that the SEEs are stochastic effects. The single particle impacting the device has a probability of causing such an event or not, and if it does not, the device will have no memory of the passage of the particle. This stagnation involves that, defined $P(t, t_0)$ the chance to go in failure, during a time t from instant t_0, $P(t, t_0) = P(t, t_0 + \Delta t)$. So a continuous maintenance cannot prevent or reduce errors. Moreover, typically in a device only a small part is SEE sensitive. The key feature to predict sensitivity or not for this type of error is the rate of occurrence.

Regarding TDEs, the effects are cumulative and can only be seen after the device is been exposed to radiation for some time and consequently periodic maintenance can help to cope with these effects. Furthermore, TDEs hit the device uniformly and in this case the most important feature is the maximum drift of parameters of interest. Radiation effects can also be distinguished depending on whether they include ionization or not (for example they might include displacement damages.

The effects that can be generated by ionization are:

- charge build-up in insulating layers (cumulative effect);
- charge injection into sensitive nodes (single ionizing event effects).

The effect that can be generated by atomic displacement is the accumulation defects in the lattice/bulk (cumulative effects).

Ionization effects depend on to the target material, since the produced charge by a given dose depends on its electronic properties and crystal structure. Therefore, the ionizing dose must be referred to a specific absorber. Displacement damage depends on the non-ionizing energy loss (NIEL), [3], i.e., the energy and momentum transferred to the lattice atoms, which exhibits a strong dependency on both particle type and energy. For this reason, the measure of displacement damage must be based on specific particle type and energy.

The most used transistor in electronic circuits is the metal oxide semiconductor field effect transistor (MOSFET). Below we will report some fundamental concepts on this type of device that will be useful for our dissertation.

There exist two different types of MOSFET: n-channel (NMOS) and p-channel (PMOS). In what follows we will focus on NMOS. For PMOS a similar treatment can be made by exchanging p with n and vice-versa.

NMOS is build on a die of silicon doped p, this part of the device is called bulk (Fig.1.3). In the bulk are generate two docks doped n, one is called “Source” and the other-one is called “Drain”. Between them there is a zone called channel. On the channel it is placed a layer of oxide (insulating layer) and on top it is placed a metal layer this junction that is called gate. The thickness of oxide layer is called t_{OX}. If we got null voltage on gate the structure become two opposed diodes in series, so no current can pass. The main idea is that by applying a voltage on gate with respect to the source electric field generates a zone with an inversion of polarity of carries an area of the bulk and an N-type channel is thus formed which allows the passage of charges as shown in (Fig.1.4). This is the so-called n-channel. This process happens because gate and channel zone form a capacitor where oxide works like dielectric, the voltage on the gate induces charge on the channel and if this charge is enough then we got the inversion of polarity and so

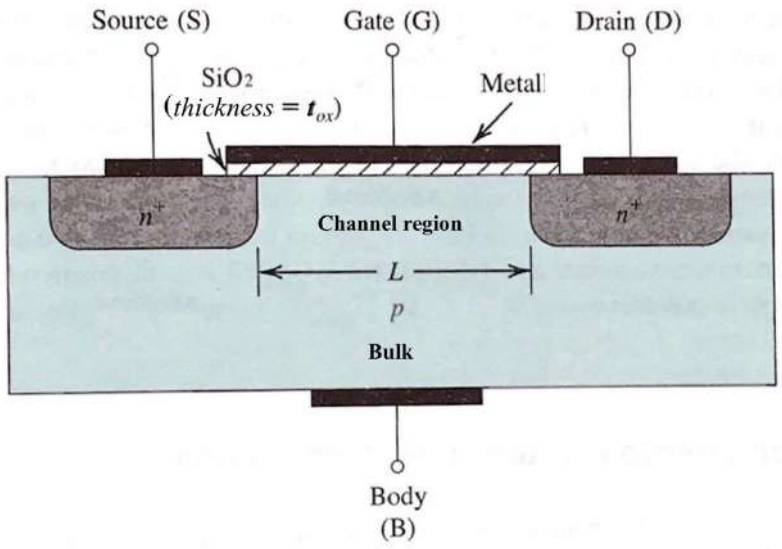

Figure 1.3: MOSFET Structure. The structure is made by a bulk and two doped regions, called drain and source, doped differently by the bulk, in the zone on between these two docks is placed a layer of oxide (insulating layer) and on top of it a metal layer that form the gate.

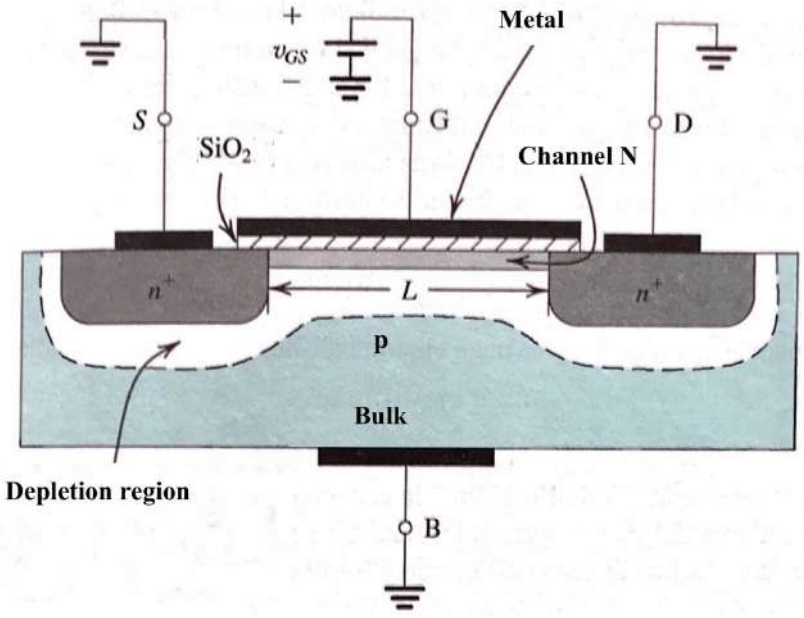

Figure 1.4: Polarization of NMOS. The figure shows the mechanism how works the channel N. The gate voltage form the conductive channel.

the current is free to pass between source and drain.

The capacity for unit of surface is given

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}. \tag{1.1}$$

If V_{DS} is the potential difference between drain and source and V_{OV} is voltage of overdrive then the current that passes between source and drain is

$$i_D = \mu_n C_{OX} \left(\frac{W}{L}\right) \left(V_{OV} - \frac{1}{2} V_{DS}\right) V_{DS}, \tag{1.2}$$

where μ_n is the mobility of the particles (electrons for n-channel, protons for p-channel), W and L are respectively width and length of the channel.

For small values of V_{DS}

$$i_D = \left[(\mu_n C_{OX} \left(\frac{W}{L}\right) V_{OV}\right] V_{DS}. \tag{1.3}$$

1.3 Total-dose effects

Before proceeding, we have to introduce the following concepts:

- Fluence: it is the number of impinging particles per unit area:

$$\Phi = \frac{N}{S} \quad \left[\frac{p}{cm^2}\right]. \tag{1.4}$$

- Flux: it is the fluence per unit time:

$$\phi = \frac{\Phi}{\Delta t} \quad \left[\frac{p}{cm^2 s}\right]. \tag{1.5}$$

- Average energy loss:

$$-S = -dE/dx \quad [keV/\mu\, m]. \tag{1.6}$$

- Stopping power: the average energy loss per unit path length of a particles. It depends on material, particles energy and particles type.

- Linear Energy Transfer (LET): it is the energy deposited per unit length by ionization, it depends on material, particles energy and particles type.

- Cross section σ: it is a parameter used to describe a process of interaction between particles and device

$$\sigma = \frac{N}{\Phi}. \tag{1.7}$$

- The radiation dose (d) is the energy deposited per unit mass, i.e. it is defined by

$$d = E/m, \tag{1.8}$$

  with E= energy, m=mass.

  It is important for cumulative effects. There are two main types of doses:

  - Total Ionization Energy Loss Dose (TID), linked to LET.
  - Displacement Damage Dose (DDD), linked to Non-Ionization Energy Loss (NIEL)Dose.

Finally, we can define the stopping power as the average energy loss for unit of density

$$S/\rho = LET + NIEL_{Coulomb} \quad [MeVcm^2/mg], \tag{1.9}$$

where ρ is density of the material, $\text{NIEL}_{Coulomb}$ is the NIEL due only by Coulomb potential.

1.3.1 Displacement damage

Displacement damage can happen from the level of a single atom up to huge clusters. Typically it is due to a particle hitting other particles thus changing the lattice structure. A particle can move an atom from its original position. We classify the damage in three categories (Fig.1.5):

- Vacancy: it is a type of point defect in a crystal where an atom is missing from one of the lattice sites.
- Interstitial: it is where an atom of the same or of a different type, occupies a normally unoccupied site in the crystal structure. When the atom is of the same type as those already present they are known as a self-interstitial defect.
- Frenkel Pair IV: it is the defect forms when an atom or smaller ion (usually cation) leaves its place in the lattice, creating a vacancy and becomes an interstitial by lodging in a nearby location.

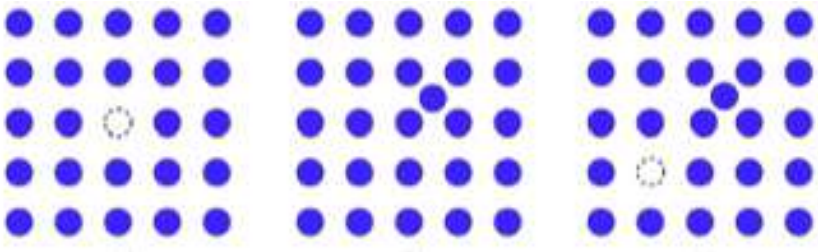

Figure 1.5: Visualization of lattice defects. Left, vacancy. Center, interstitial. Right, Frenkel Pair IV.

The band structure changes following a periodicity break in the crystal lattice of a generic Si-based device (Fig.1.6).

The incident original particles hit an atom, the so called Primary Knock-on Atom (PKA), which can generate cascades (nuclear elastic) and sub-cascades (nuclear reactions), the atoms displaced by the PKA are called Secondary Knock-on Atoms (SKA), and this nomenclature can be extended to tertiary (TKA) and

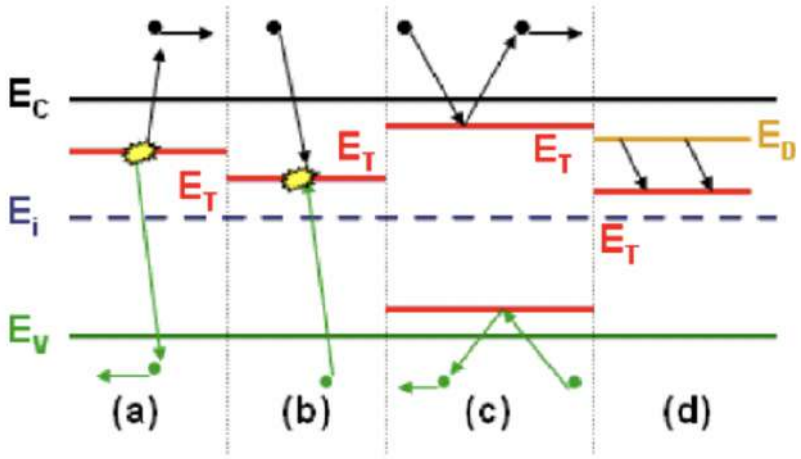

Figure 1.6: Band structure of silicon after undergoing trap states in the lattice due to displacement damage.

so on. In the Figure 1.7 we can see that the cascade may be generated for particles with energy higher than 1-2 KeV and for energy higher than 12-20 KeV we can have sub-cascade.

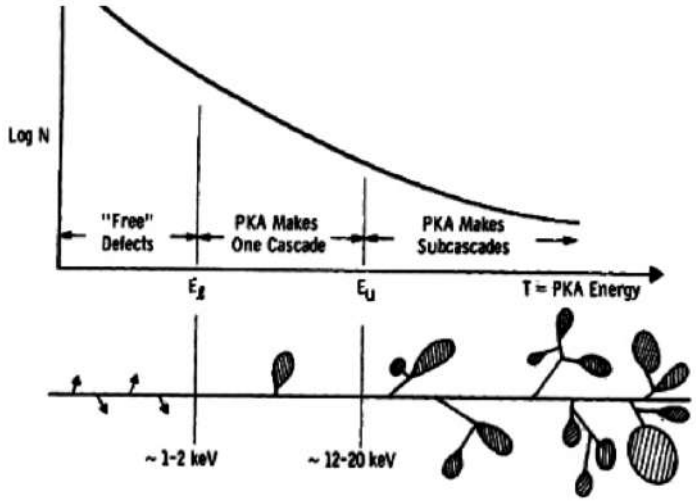

Figure 1.7: PKA cascade effects as a function of the energy of the PKA.

The PKAs, SKAs and TKAs may generate ionization and lattice defects such as vacancy, interstitial or Frenkel pair defects.

What we have seen so far represents the main damage mechanism in silicon and becomes significant in conductor devices (e.g. BJT and JFETs). the probability of damage being generated is strongly linked to Non-Ionizing Energy Loss (NIEL)

The NIEL as shown in the figure depends strongly on the type and energy of the particles (Fig.1.8).

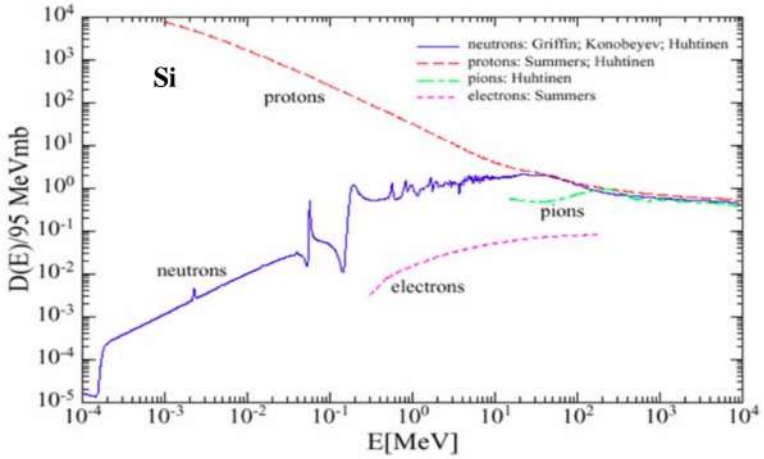

Figure 1.8: Displacement damage function in Si as a function of the energy for different particles. Source [4].
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Figure 1.8 shows the displacement damage function D(E) [MeV mb] in Si as a function of the energy for neutrons, protons, pions, and electrons, plotted relative to 1 MeV neutrons [5].

D(E) is directly proportional to NIEL, i.e., it is

$$\mathrm{D}(E) = \frac{A}{N_A} NIEL(T_0), \tag{1.10}$$

where T_0 is the energy of the incident particles, A depends on materials and

$$NIEL = \frac{N_A}{A} \int_{T_{min}}^{T_{max}} \mathrm{d}T\, Q(T)\, T \left(\frac{\mathrm{d}\sigma}{\mathrm{d}T}\right)_{T_0}, \tag{1.11}$$

where Q(T) is the partition factor which gives the fraction of T to be lost to NIEL and $\frac{\mathrm{d}\sigma}{\mathrm{d}T}$ is the differential partial cross section for creating a given recoil with energy T, T_{min} is the minimum energy transfer and T_{max} is ones maximum.

We can see that over an energy of 50 MeV protons and neutrons have a similar D(E), it is an important feature we will face later in this thesis. The displacement

damage can be mainly observed through three types of modification of the crystals bound states.

1.3.2 Ionization Damage (Total Ionizing Dose)

The other category of possible problems is ionizing damage. This issue occurs when a particle impacts and creates hole electron pairs. It is possible to have this type of effect both in the insulators and in the semiconductors. This $e-h$ pairs can be diffuse or drift (if there is an electric field) in the device and they may get trapped. The number of pairs formed is proportional to the energy that has been absorbed and consequently the damage is closely related to the dose. This effect is not symmetrical between electrons and holes (Fig.1.9): electrons drift toward the gate quickly, high mobility ($\mu_e = 20\, cm^2\, V^{-1}\, s^{-1}$) and holes drift towards Si/SiO_2 interface (μ_h = from 10^{-4} to $10^{-11}\, cm^2\, V^{-1}\, s^{-1}$), through trap hopping (Fig.1.10):

$$\Delta V_{OT} = -\frac{Q_{OT}}{\epsilon_{OX}} t_{ox}, \tag{1.12}$$

$$\Delta V_{IT} = -\frac{Q_{IT}}{\epsilon_{OX}} t_{ox}, \tag{1.13}$$

where C_{ox}= oxide capacitance per unit area, Q_{OT}= charge trapped in the oxide per unit area, Q_{IT}= charge trapped at the SiO_2/Si per unit area.

The energy required to form a pair is 18 eV in SiO_2 ([6]).

The ionization damage can be quantified through:

- interface trapped charge;
- oxide trapped charge;
- the mobility of trapped charge;
- the time and voltage dependence of charge states.

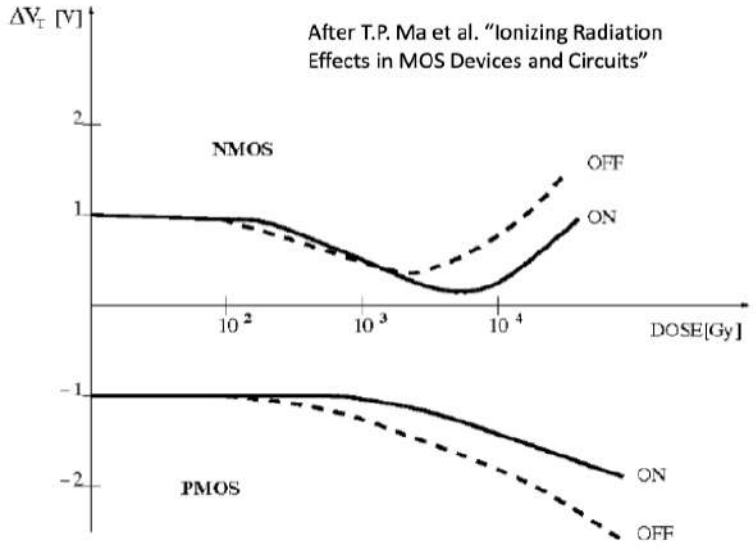

Figure 1.9: Ionizing Radiation in PMOS vs NMOS.

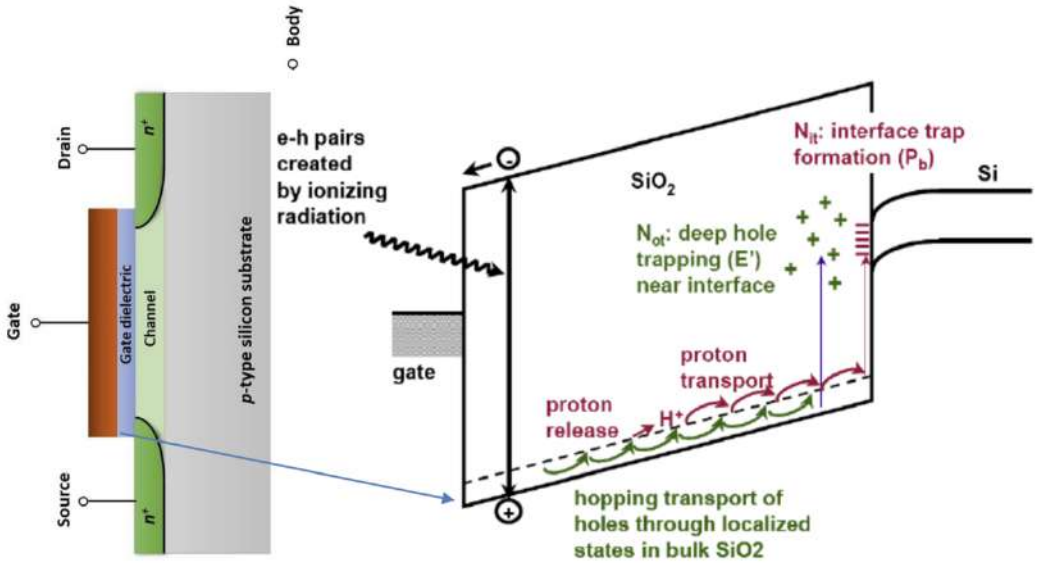

Figure 1.10: MOSFET structure. Trapping mechanism in SiO_2.

1.3.2.1 V_t shift

The first effect we are going to analyze is called V_t shift in MOSFETs, where charges are trapped in the silicon layer which in a MOSFET transistor represents the oxide surface on which the two opposite doped areas and the gate are positioned. Whether they are P-MOS or N-MOS transistors, different charges remain trapped (due to the difference in electric potential that is present in the transistor itself). For those concerning trapping effect, there exists an asymmetry between P-MOS or N-MOS (Fig.1.9).

It is quite intuitive that being an effect linked to the absorbed dose, the smaller oxide thickness is, the lower he suffers. The fact that technological progress is leading these oxide thickness to be smaller and smaller mitigates of this effect. The amount of recombination depends on the fractional charge yield, which is a function of the applied electric field and on the type and energy of the incident radiation; The amount of recombination is well established for thermally grown silicon dioxide, while much less is known for other dielectrics, like SiN, which are largely used in the microelectronic industry. Along with the electron-hole generation and/or hole transport processes, chemical bonds in the oxide structure may be broken; in particular, bonds associated with hydrogen (H^+) and hydroxyl groups (OH^-) may release hydrogen ions (protons), which may migrate to the Si/SiO_2 interface and undergo a reaction resulting in the creation of interface traps; also defects created in the oxide bulk can migrate and form interface traps. So it is important look at the hole transport mechanism. The Figure 1.11 shows that the phenomena start with an initially empty localized trap a): when a hole, while moving through the oxide, gets stuck in it, the total energy of the system is lowered by a distortion of the lattice around the trap site b), the hole digs a potential well for itself, i.e., it is self trapped. The transition of the trap between two nearby sites occurs via an intermediate thermally activated state c), for which thermal

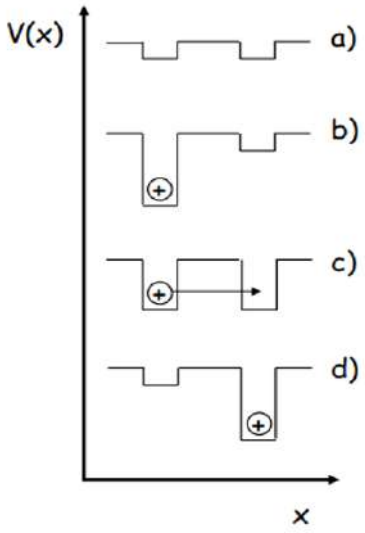

Figure 1.11: Hole transport mechanism.

fluctuations of the system momentarily bring the electronic energy levels very close to each other; the hole tunnels from the first to the second site. In the final state of the process, the hole resides in the second site d), the transition probability depending on the tunneling transition probability and on the probability that the intermediate state in c) is created (Fig.1.11).

Oxide charge trapping and interface trap buildup induced by ionizing radiation also are responsible for a remarkable change in the ID-VGS curves in MOSFETs, two different effects can be distinguished (Fig.1.12): a shift of the curve along the voltage axes (towards negative values for NMOS, towards positive values for PMOS transistors) due to threshold voltage shift; a decrease in the sub-threshold curve slope (curve stretch-out) for both device types, which was experimentally found to be correlated to interface trap buildup. As a consequence of these effects, a net increase in the NMOS drain current is observed at VGS=0, while no increase (if not a decrease) can be detected in the PMOS (Fig.1.13). The second effect we are going to analyze is called annealing. The annealing process in MOSFETs involves complex mechanisms related to the interfaces and different materials characterizing the total structure. Among them, the holes detrapping

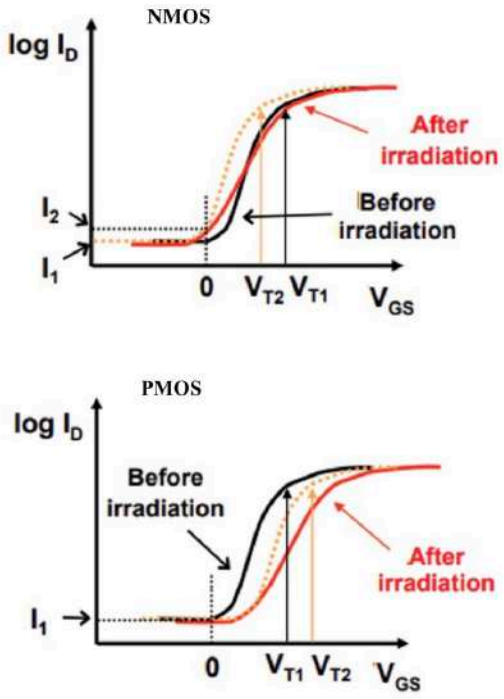

Figure 1.12: The effects of total dose on the response of silicon device. Drain currents vs state voltage in a NMOS (top) and PMOS (bottom).

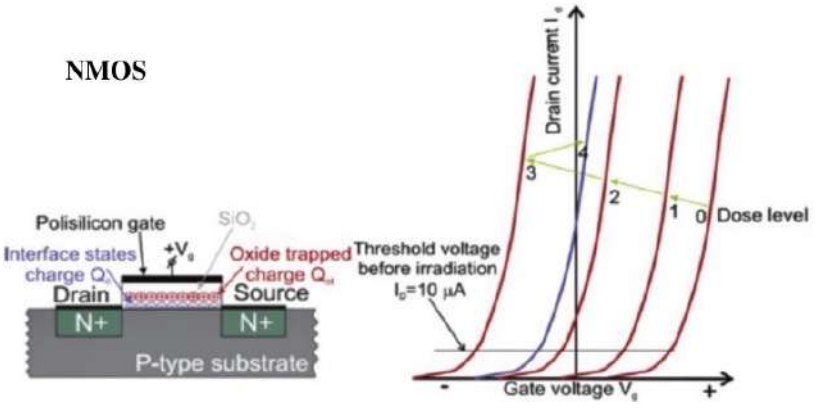

Figure 1.13: Change of threshold voltage due to radiation.

from the Si/SiO_2 interface constitutes the main contribution to the long-term annealing of the radiation damage occurring near room temperature. In general, the holes move away from the traps via recombination with the electrons transferred from the conductive channel. This can occur in two ways: tunnelling and thermal diffusion. The tunneling model assumes the recombination between the tunnelled silicon electrons and the holes distribution near the Si/SiO_2 interface. It correctly predicts the slow bias-dependent recovery of the threshold voltage variation at normal operating temperatures (between -55° and 125°). The recombination depth depends on the tunnelling barrier height and, in general, the time. As far as the thermal recombination, the normal operation temperatures give enough kinetic energy to SiO_2 valence electrons, allowing the recombination with the trapped holes. As expected, this phenomenon is favored as long as the energy difference between traps levels and valence band is small and the temperature is high.

1.3.2.2 Rescaling effects

The trend to device scaling in the modern microelectronic industry has brought along a progressive reduction of the gate oxide thickness and an ever higher degree of tolerance to ionizing radiation. On the other hand, one method to increase radiation hardened in circuit is electrically isolate devices from each other, features a thickness ranging between 100 and 1000 nm. the main kinds of isolating oxides are used in modern CMOS processes: Shallow Trench Isolation (STI): barriers of insulating material are introduced so as to make it impossible to form PNPN structures. In an NMOS device, positive charge trapping in the field oxide due to ionizing radiation may form an N-type conducting channel between the source and drain terminals, therefore increasing the drain leakage current. Positive charge trapped in the field oxide may create a parasitic channel between the source and drain terminals under the bird's break region (Fig.1.14 a)). The oxide thickness in the bird's beak region is larger than in the gate oxide and the accumulated

positive charge can be such that the underlying P substrate is inverted and an N-type channel is created.

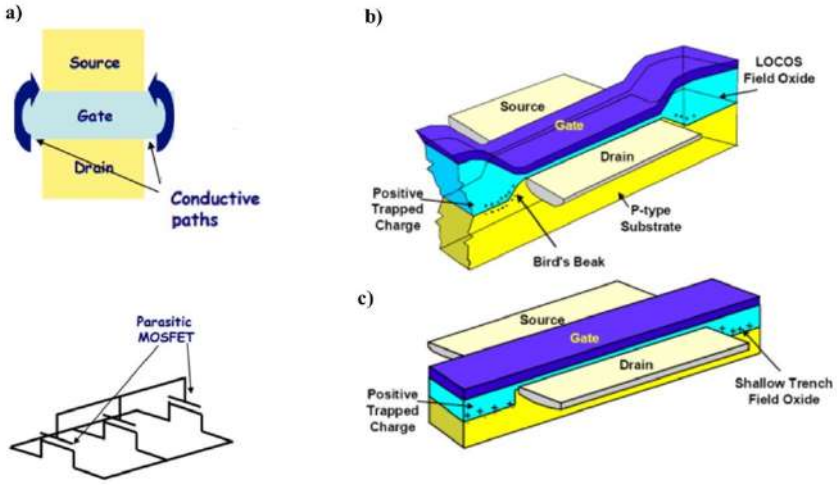

Figure 1.14: Left, Parasitic transistor in parallel a). Right, Parasitic channel between the source and drain terminals b) NMOS, c) PMOS.

The radiation induced channel can be modeled with a parasitic transistor in parallel with the main device and featuring a different width W but the same length L. This effect can be observed only in NMOS transistors (Fig.1.14) since in PMOS devices the charge in the channel is carried by holes The gaps trapped in the oxide give rise to a negative variation ΔV_{OT} of the threshold voltage.

$$\Delta V_{OT} = -\frac{q}{C_{OX}}\Delta N_{ot} = -\frac{q}{\epsilon_{OX}} t_{OX} \Delta N_{ot}, \tag{1.14}$$

where ΔV_{OT} and q are defined as in paragraph 1.3.2, ϵ_{OX} is the dielectric constant of the oxide and ΔN_{ot} is the density of gaps trapped in the oxide.

It is then possible to address the issue by changing layout (Fig.1.15), shortly the main idea is avoid the areas where this charges converge, these are specific area (edges), so if we build a transistor with shape of a ring with in the center the drain we totally avoid this issue.

Shortly, the radiation-induced threshold voltage shift effect has been gradually

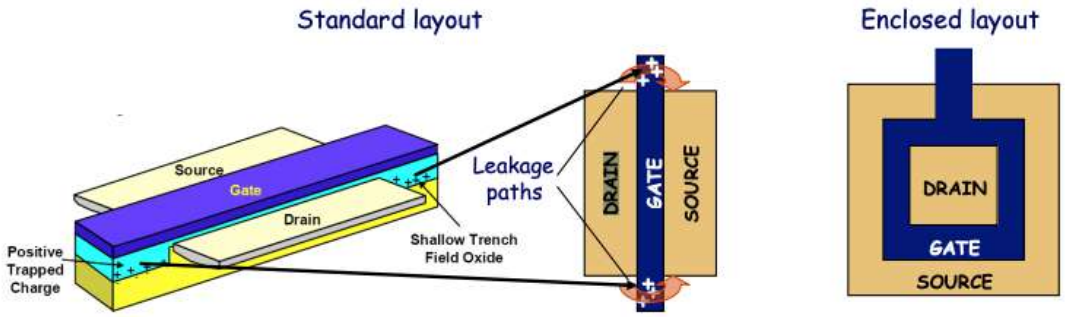

Figure 1.15: Left, center 3D view of MOSFET with trapped positive charge. Right, enclosed-layout transistor (edge-less).

mitigated by the natural evolution of advanced microelectronic technologies, where the gate oxide thickness has been reduced generation after generation (Fig.1.16).

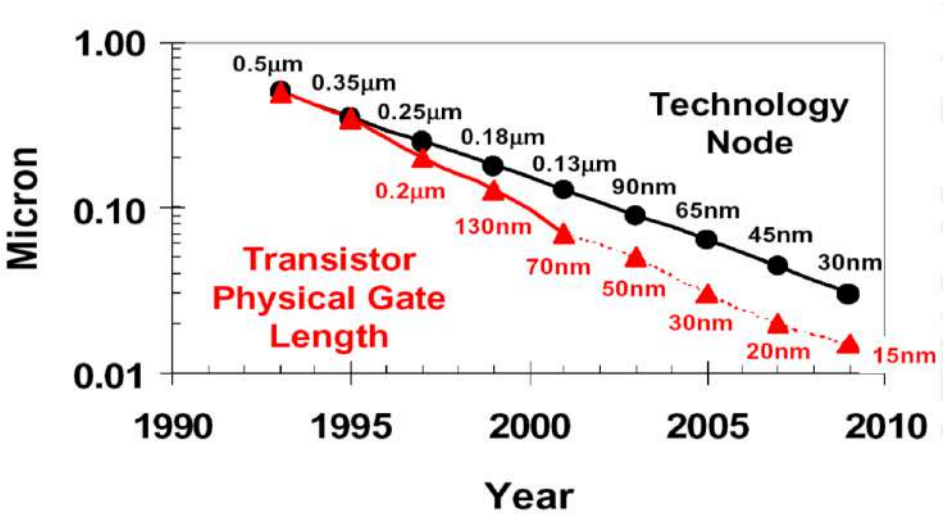

Figure 1.16: Evolution during time of the feature size of MOS device.

Now the main radiation hardness issues in microelectronic circuits are those relevant to the isolating structures , affecting both static and noise properties of MOSFET devices, together with single event effects (Fig.1.17).

Gate oxides with dielectric constant larger than in SiO_2 (High-K oxides) will be used to reduce the gate leakage current; on the other hand, such new dielectric materials still need to be appropriately tested from the standpoint of radiation-tolerance.

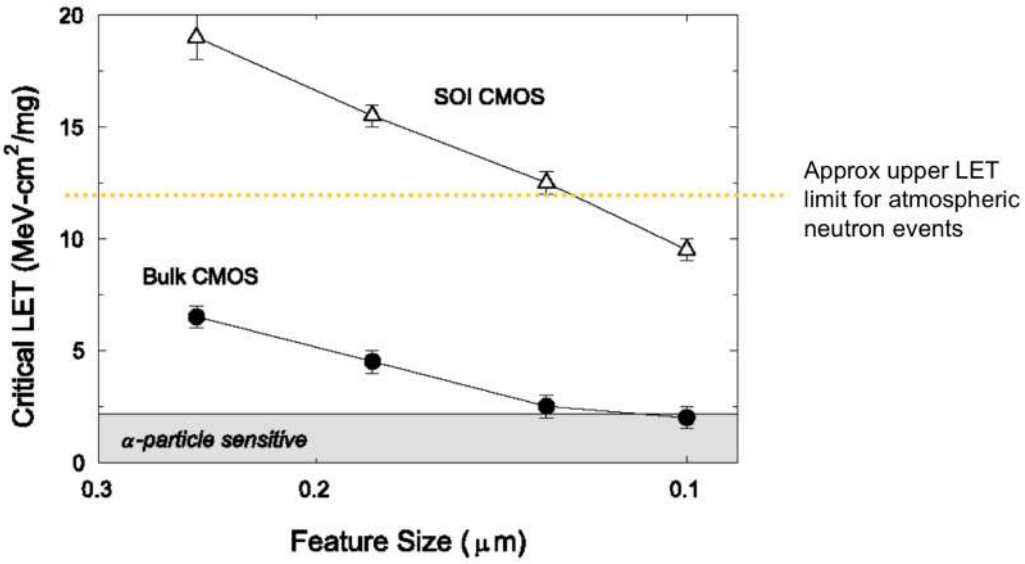

Figure 1.17: Feature size vs critical LET.

1.4 Single event effects

Ionization induced by a single particle crossing a sensitive device area can cause Single event effects (SEEs). The critical LET or threshold LET (LET_{th}) is defined as the minimum LET value causing this single event effect.

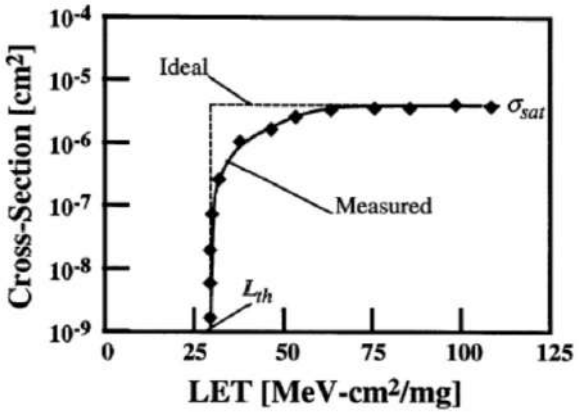

Figure 1.18: LET vs SEE cross section plot.

The SEE cross section fit function is

$$\sigma(LET) = \sigma_{sat}\left(1 - e^{\left(-\frac{LET - LET_{th}}{W}\right)^S}\right), \tag{1.15}$$

where σ_{sat} is the saturation cross section, W and S are fit parameter (Fig.1.18).

In general, new technologies are increasingly sensitive to SEEs, in fact they only occur when the particle impacts certain sensitive areas in the device, smaller devices have smaller capacitance, increasing the effects of charges injected from the outside.

Another important features bring with rescaling is that the voltage that occur in new (and smaller) transistor are lower, so it is easier for a particle to release enough charge to cause a failure (Fig.1.19).

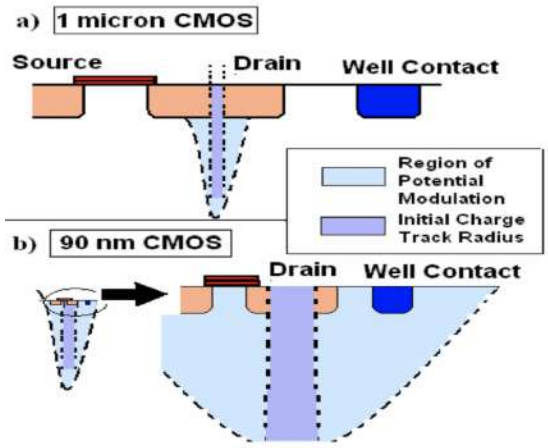

Figure 1.19: Impact of scaling on radiation effects. (a) Effect of ion impact on 1μm CMOS. (b) Effect of ion impact on 90 nm CMOS. Source [7].

The types of SEEs can be summarized as in Fig.1.20. They will be commented in detail later for each type.

1.4.1 Soft-errors

Soft errors are those events that cause momentary malfunctions of the device, in some cases they can have no real effects and same types of them. Some techniques make the circuits capable of correcting this type of errors autonomously, i.e., a very well designed state machine that falls into an illegal state is capable of getting out of it autonomously, or, in the worst case, a reset of the device is enough.

The single-event transient is voltage spike at a node in an integrated circuit.

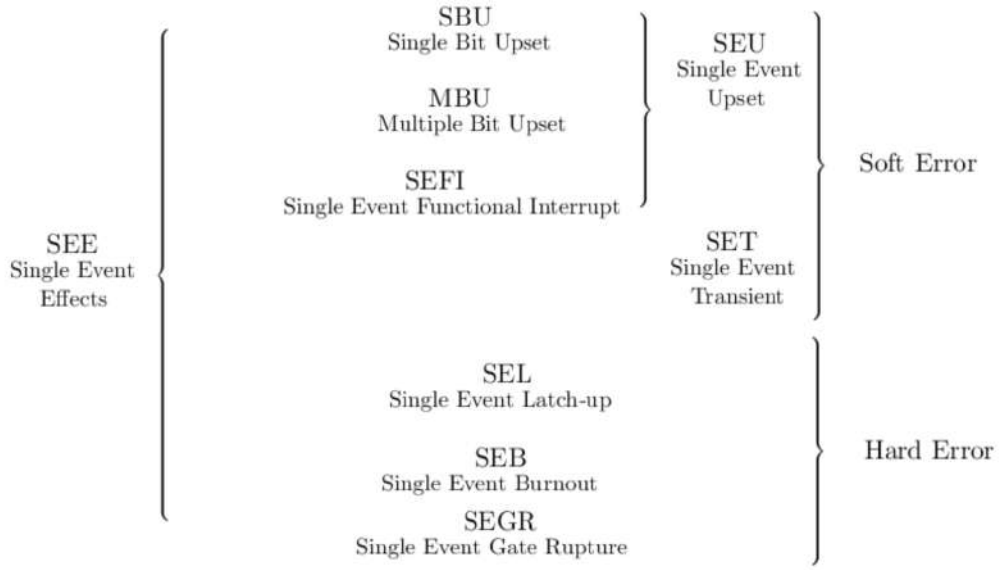

Figure 1.20: Errors scheme.

It is normally formed by the electric field separation of the charge generated by an ion passing through or near a junction. In CMOS transistors in OFF state, drain and substrate are reverse-biased PN junctions. As shown in Fig 1.21, at the onset of an ionizing radiation event, a cylindrical track of electron hole pairs with a submicron radius and a very high carrier concentration is formed in the wake of the energetic ion's passage (a). When the resultant ionization track traverses or comes close to the depletion region, carriers are rapidly collected by the electric field creating a large current/voltage transient at that node (b). This "prompt" collection phase is completed within a nanosecond and followed by a phase where diffusion begins to dominate the collection process (c) [8]. Additional charge is collected as electrons diffuse into the depletion region on a longer time scale (hundreds of nanoseconds) until all excess carriers have been collected, recombined, or diffused away from the junction area. The corresponding current pulse resulting from these three phases is also shown in Fig.1.21. Charges, released by gaps, move in the semiconductor under the influence of the electric field through the semi-

conductor drift and diffusion processes. This charge movement results in voltage transients between drain and source (Fig.1.22).

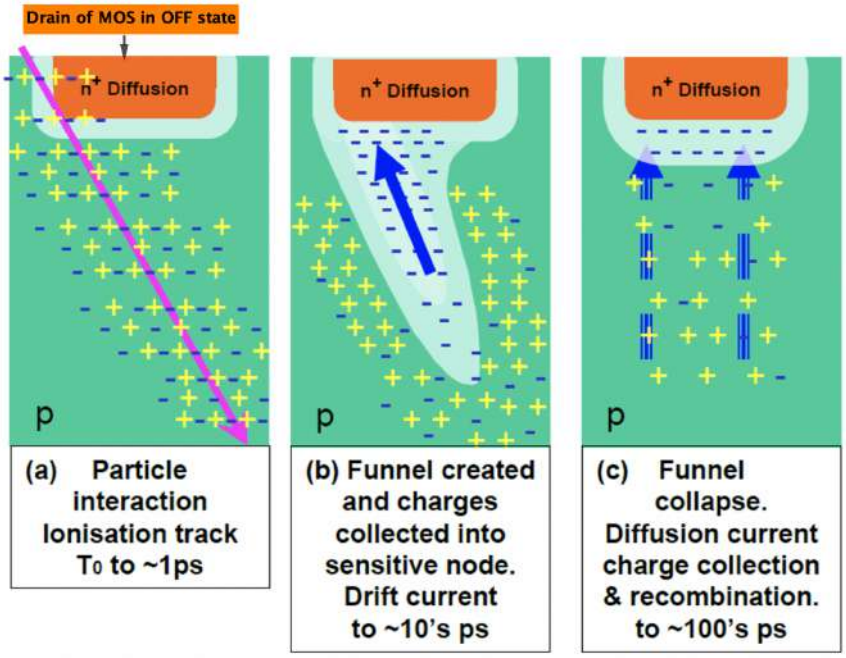

Figure 1.21: Single event transient scheme.

The single-event upset is a change of state of memory cells. It occurs when a charged particle causes a single-event transient in a device port of a memory cell, port of feedback loop.

The output will depend on where this switch took place (Fig.1.23). At time t_0 if a charge is injected into transistor Q_3 it goes from OFF to ON, then at time t_1 transistors Q_2 and Q_4 will change state and at time t_2 memory cell return to a stable situation but which will have different content in the memory cell.

The single-event functional interrupt (SEFI) is a condition where the device stops normal functions, and usually requires a power reset to resume normal operations. It is a special case of single event upset (SEU) changing an internal control signal. It may happen in complex components like central processing units (CPUs) and FPGAs [10].

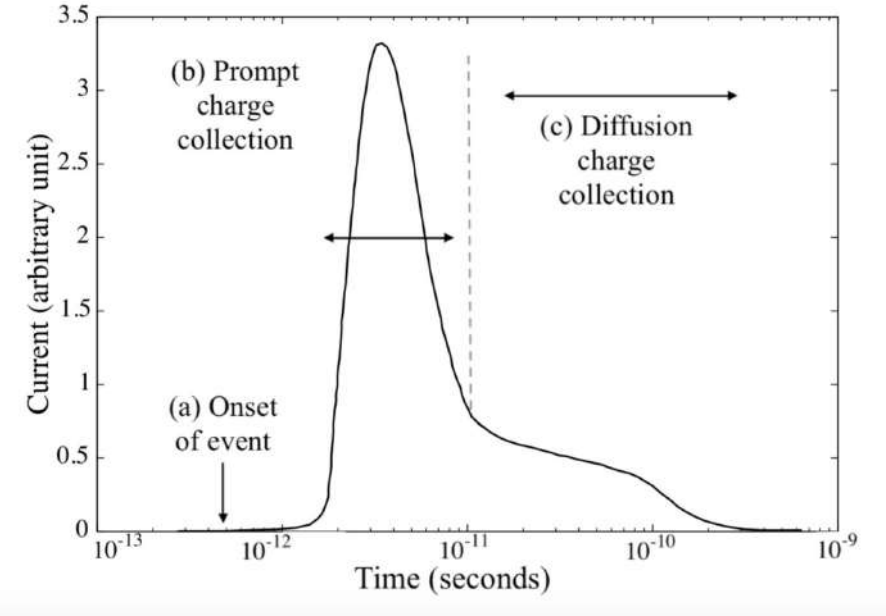

Figure 1.22: Current peak plot due to SET. Source [9].

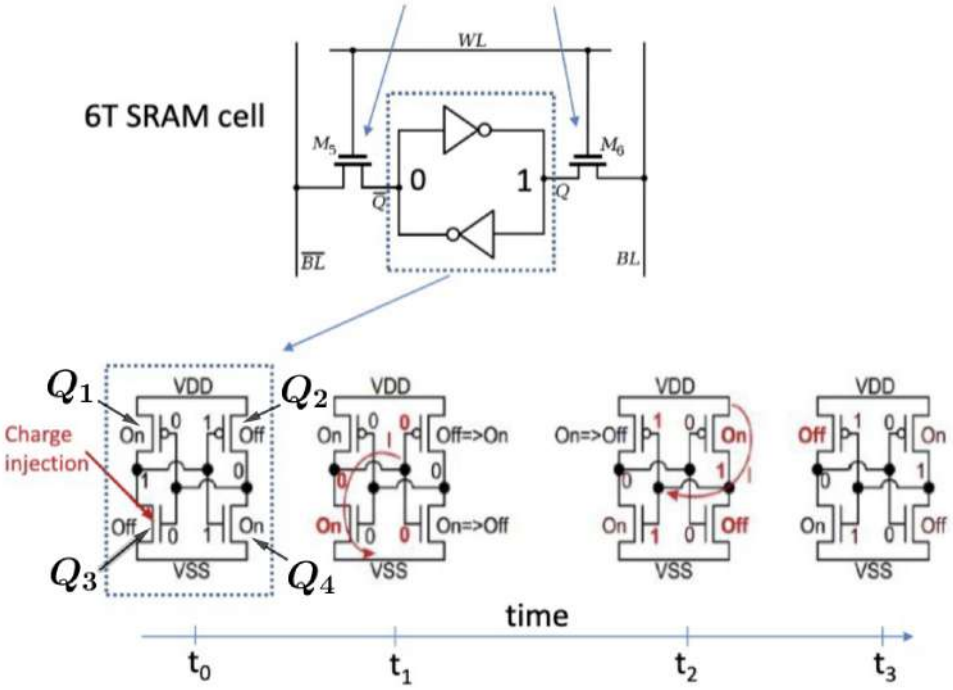

Figure 1.23: Upset generation process.

1.4.2 Hard-errors

Hard errors are a form damage to the device that is unrepairable these processes remain even after a power cycle of the device.

The single-event gate burnout happens when an ion strike can turn on a real bipolar junction transistor (BJT) or a parasitic BJT structure in a (usually) NMOS. The resulting second breakdown causes a high-current state and can cause thermal failure of the device. Due to particle strike, the substrate right under the source region gets forward biased, and the drain-source voltage is higher than the breakdown voltage of the parasitic structures. The resulting high current and overheating may then destroy the device. MOSFETs, BJTs, and some CMOS structures are very susceptible to single event burnouts (see [11],[12] and Fig.1.24).

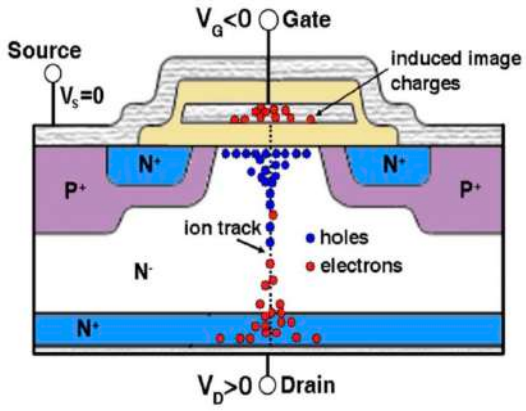

Figure 1.24: Single event gate rupture in power MOSFET.

The single-event gate rupture is a local breakdown that happens in the insulating layer of SiO_2, causing local overheating and destruction of the gate region (see [13]). Single event gate rupture only affects transistors when they are in their nonconducting states (VGS<0V for n-channel devices or VGS>0V for p channel devices). In the case of single event gate rupture, holes from the ion strike pileup under the gate, thus increasing the electric field across the MOSFET gate oxide to its dielectric breakdown point. The resulting flow of the current causes thermal

failure of the gate oxide. These events represent localized breakdowns in the oxide and also can result in latent damage.

The single-event latch-up is the activation of parasitic bipolar devices in a CMOS integrated circuit. The result is a low-impedance path from the chip power supply to ground, due a parassitic PNPN structure build in MOSFET. Injection of charge in this loop might trigger a self-amplifying current, a low impedance path between VSS and VDD may generate a permanent failure of the component. Latch-up is a potentially catastrophic condition where a low resistance path develops between power supply and ground on a device that remains after the triggering event is removed (Fig.1.25).

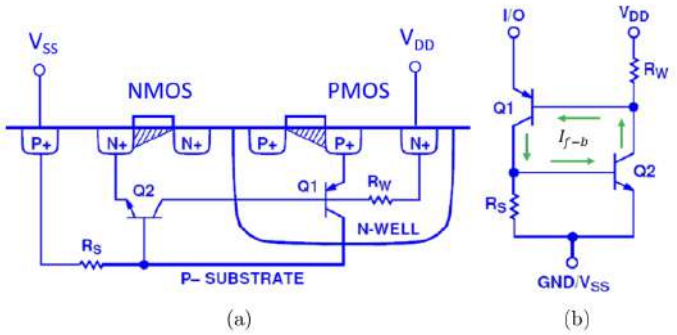

Figure 1.25: Parasitic PNPN structure in CMOS (a). The PNPN parasitic structure represented through two bipolar transistor.

When currents are sufficiently high metal traces can vaporize, bond wires can fuse open, and silicon regions can melt down due to thermal runaway. Once latched, this high current condition will continue until power is removed from the device or it fails catastrophically. While latch-up is troublesome in ground-based systems and can result in low system reliability and expensive repairs, it can be disastrous in space-based systems leading to system failure and often the loss of an entire mission at a significant cost. Latch-up dates back to the development of the thyristor switch first conceived by Shockley and Ebers in the early 1950s (see [14], [15]). The detailed principles of operation and first working device were developed by Moll in 1956 [15].

Therefore, very short duration pulses cannot trigger the parasitic PNPN structure because the devices are not fast enough to respond. However, with device scaling the parasitic thyristor's frequency response also improves, meaning it becomes more sensitive to short duration pulses prevent latch-up prevention stay below the absolute maximum ratings of the chip. The NMOS and PMOS devices are isolated by using an oxide trench together with a buried oxide layer (Fig.1.26).

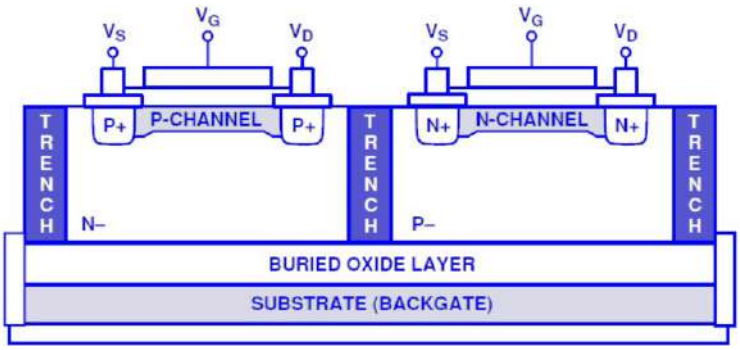

Figure 1.26: Shellow trench isulations as solution to avoid PNPN.

In the next chapter, we will talk about such tools and present some examples of where they are used. In particular, we focus on Hadron Fluence Sensors.

Chapter 2

Hadron Fluence Sensors

2.1 Radiation sensors for electronics protection

Failure of electronic equipment due to radiation is a severe problem for particle physics experiments at colliders. In fact, particle beams are used to produce collisions, either beam-beam or beam-target in physics experiments and the instruments near them are exposed to radiation. For this reason, there has been a growing awareness over the years of the need to consider radiation immunity as constraint in experimental design.

For electronics, failures can occur due to for three main reasons: TID, NIEL, and SEEs, and these different effects are monitored by their pertaining sensors, [16]. The RadMon system includes RadFETs for Total Ionising Dose (TID) measurements, silicon p-i-n diodes for the 1-MeV equivalent neutron fluence, and SRAM memories for the high energy hadron and thermal neutron fluence. RadMon system has been developed by the CERN ENgineering (EN) department [17]. As far as radiation monitoring systems are concerned, radiation can be decomposed into three physical parameters, which are independent and represented as orthogonal in Fig.2.1.

Fig.2.1 illustrates the relationship between different types of radiation and their

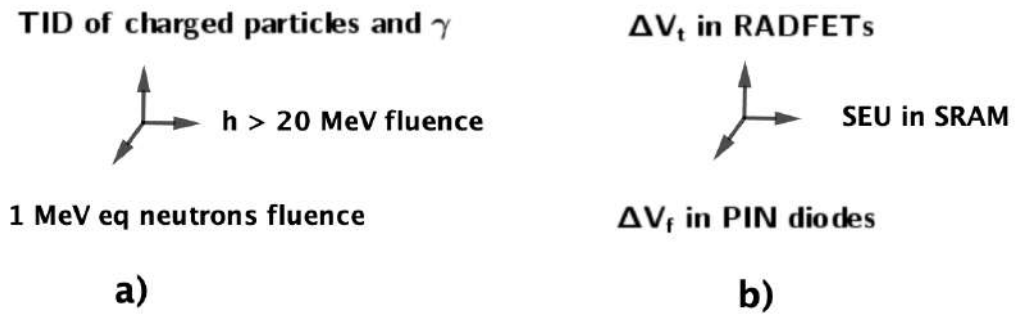

Figure 2.1: The radiation types and the associated type of radiation damage and radiation sensor

effects on electronic devices and pertaining radiation sensors.

2.1.1 Total ionizing dose sensors

TID sensors are used to control the radiation effects on the electronic components. They are required to be low-power, compact, highly accurate. TID sensors are also widely used in research physics facilities, such as charged particle accelerators, where a wide operating range is required to measure the dose rate and total dose of ionization radiation. Dose causes TID, which can be detected by so-called radiation-sensitive field-effect transistors (RADFETs), based on metal-oxide-semiconductor (MOS) processes.

These devices are simple, low-power, low-cost, and do not require complex electronics connections to process the measurement results. RADFETs are usually made with thick gate oxide (typically $>$ 100 nm) to increase sensitivity to total dose. In operation 0.07 mV/Gy(Si) sensitivity was achieved by means of RADFET with thick oxide. They are used in environments where the expected radiation consists of charged particles but can be also used to detect gammas ray-dose[18].

2.1.2 Non-ionizing energy loss sensors

Many studies ([19], [20], [21] and [22]) have successfully shown that the degra-

dation of semiconductor devices in a radiation field can be linearly correlated to the displacement damage energy, followed by the non-ionizing energy loss NIEL deposited in the semiconductor devices. The NIEL sensors are used to predict radiation damage and survivability of components in radiation fields, such as the detectors used at the LHC at CERN. Neutrons, protons, charged hadrons and ions cause NIELs.

Information about incident neutrons can be obtained by measuring the radiation emitted by a material whose radioactivity is induced by interaction with neutrons. Such detectors are called activation detectors. The usage of these detectors to measure neutron radiation is limited [23] due to radiation protection constraints.

Detectors used in high-energy physics (HEP) experiments often operate under high particle-flux environments, which are required to obtain the large statistical samples needed to characterize rare physical processes. For example the detectors at the Large Hadron Collider (LHC) at CERN accumulate radiation over time and TID for the innermost pixel sensors is expected to be about 300 kGy over the expected lifetime of the instrumentation. For the High-Luminosity LHC (HL-LHC), the upgrade of the LHC to be commissioned to operation in 2026, a factor-10 higher integrated luminosity of 4000 fb^{-1} with proportionally higher radiation levels is anticipated. In comparison to radiation fields encountered in space applications, the displacement damage effects, in high luminosity accelerator experiments are higher by orders of magnitude. Therefore, the radiation fields in the experiments of the LHC are unique in terms of intensity and composition. While results obtained in the low particle fluence region for non-HEP applications can be partially applied to HEP, the operation of semiconductor devices in the high fluence range has called for dedicated R&D programs. The aim is to understand the displacement damage effects on semiconductor devices, especially silicon detectors, and to develop targeted radiation testing campaigns and techniques to

assure adequate performance over decades of operation in the harsh radiation environments of the experiments [24]. A recent book related to displacement damage in silicon devices for HEP applications has been published by Hartmann [25].

2.1.3 SRAM-based hadron fluence sensors

When an SRAM memory cell is exposed to ionizing radiation, the energy deposited by a single ionizing particle may be sufficient to change the state of the memory cell (SEU). The number of SEUs induced in the SRAM memory is proportional to the incoming particle fluence. The ratio of number of induced SEU to the particle fluence defines the sensitivity of the memory. Hence, a SRAM memory can be utilized as radiation monitor. The sensitivity of the SRAM memory depends on the Supply voltage. Reducing the Supply voltage of an SRAM memory cell will lead to a proportional decrease in the charge stored at its sensitive node, and consequently also the critical charge that must be released by ionization to induce an . This will increase the sensitivity of the SRAM memory when operated at a reduced Supply voltage. Furthermore, the sensitivity of a SRAM memory varies according to the energy of the incoming hadron particles [17].

For example, the radiation monitors in use at CERN's Large Hadron Collider for protection of the electronics are based on SRAMs as sensitive elements for measuring fluence of high-energy hadrons (HEHs), where "high-energy" refers to E>20 MeV.

Possible applications of hadrons fluence sensors are radiation monitoring at HEP, nuclear, or space experiments, accelerators, and in medical physics (e.g. in proton therapy).

2.2 FPGA configuration memory technologies

Field programmable gate arrays (FPGAs) are digital integrated circuits configurable to perform specific logic functions.

FPGA devices are characterized by the presence of programmable routing and logic resources. This type of device is generally easier to program because many resources (i.e. clock trees) are already present on the chip and the designer only needs to work on connecting these resources to obtain a circuit. The specific hardware functions that are programmed into an FPGA are defined in a binary file, i.e., the bitstream. This file is generated following a rigorous design flow, synthesis and validation process.

FPGAs are classified according to the type of on-chip configuration memory that stores this bitstream file, typically, SRAM, Flash, and Anti-fuse [26].

Fig.2.2 shows the three types of configuration memory cells for FPGA devices.

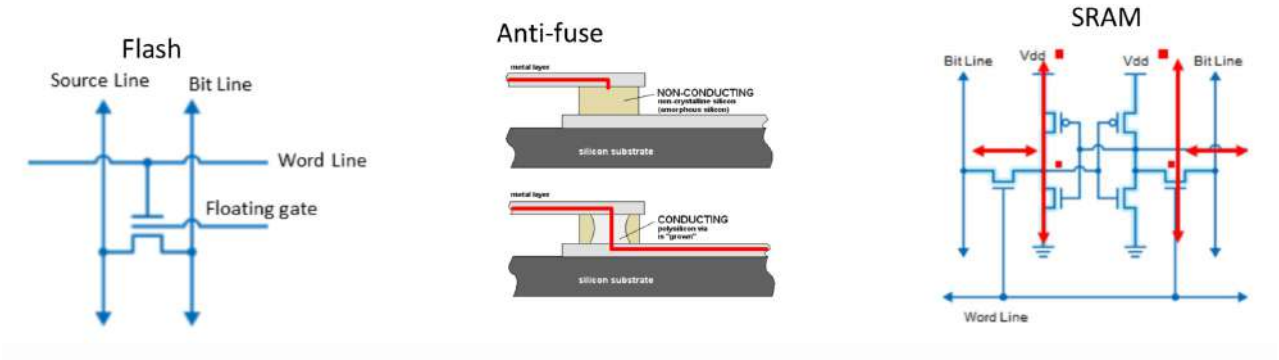

Figure 2.2: Three types available: Flash (left), Anti-fuse/fuse (center) and SRAM-based (right).

Configuration memory technology	Principali Fornitori	processo CMOS
Flash (SONOS)	Microchip (formerly Microsemi)	non-standard
Anti-fuse	Microchip (formerly Microsemi)	non-standard
SRAM	Xilinx, Inte (formerly Altera), Latticel	standard

Table 2.1: Types of FPGAs.

- Anti-fuse.

Anti-fuse devices have many modules. All of these units are simple, have predefined functions, connected with each other by means of anti-fuses. They are normally open and become short when a current higher than a threshold value flows. This type of FPGAs are therefore non-volatile, the configuration is in fact stored even when the power supply voltage is removed; however, they are one time programmable.

They present the following advantages:

a) Anti-fuses are immune to total dose and single event effects;

b) they have immediate operation at power-on;

c) they have lower propagation delays of interconnections.

They present the following disadvantages:

a) Their implementation requires non-standard CMOS process;

b) they have slower performance growth over the years compared to reprogrammable SRAM-based devices due to the lack of proprietary standards for the manufacturing process;

c) they can be programmed only one time, the functionality cannot be updated.

- Flash.

  In FPGAs built using flash technology the programmable interconnection elements are based on MOSFET transistors with floating gate used as switches Each switch is made by means of a transistor with floating-gate, typically used to store the charge; a second transistor is instead used for the read-back check of the switch configuration.

  They present the following advantages:

a) They require less resources respect to devices based on SRAM technology where they are typically used 6 transistor for each programmable item;

b) immunity of the device to SEUs, because there is no feedback structure;

c) it gives possibility to reprogram the devices, this is valuable feature in the debug phase to modify the functionalities and debug.

Flash-based FPGA's are a combination of FPGAs with flash memory, therefore, they are non-volatile and re-programmabile.

- SRAM-based FPGA.

  Over the last few years flash-based FPGAs have being considered for SRAM readout at CERN [27] and actually used in proton therapy [28]. However, these components may limit the lifetime of the radiation monitor due to their relatively low TID tolerance [29]. Possible solutions is that they require separate components for sensing upsets and for reading them out, but so the power consumption, the board complexity and its size increase.

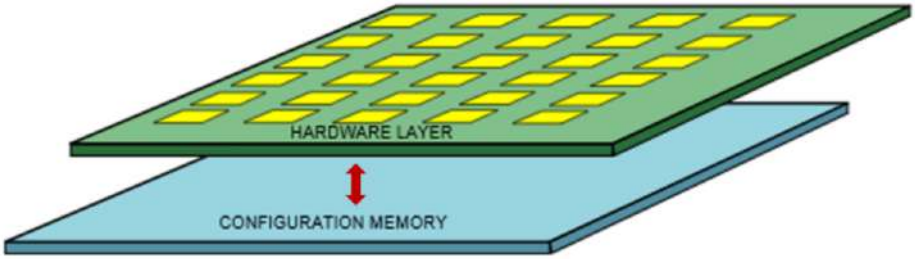

Figure 2.3: FPGA programmable logic and configuration SRAM

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They present the following advantages:

a) This technology uses a standard manufacturing process for CMOS;

b) it make it possible have high logical capacity and high level of integration;

c) it has higher operational frequency with respect to the other configuration memory technology;

d) it has lower costs with the same functionality and resources;

e) it gives possibility to reprogram the devices, this is valuable feature in the debug phase to modify the functionalities and debug.

The disadvantage of SRAMs are:

a) They have low tolerance to SEU;

b) they are volatile and therefore in order to use a SRAM-based FPGAs, at each power-up it is necessary to load the configuration from an external non-volatile memory;

c) they have a static current consumption.

In the next chapter we will discuss SEE on SRAM-based FPGAs and the solutions to mitigate SEU effects on FPGAs configuration memory.

Chapter 3

Single Event Effects and Mitigation Techniques in SRAM-based FPGAs

In this chapter we will talk about SEE and mitigation techniques in SRAM-based FPGAs. First, we will describe Xilinx FPGAs architecture.

3.1 Architecture of an FPGA

The main vendors in the world of programmable logic in SRAM technology are AMD (formerly Xilinx) and Intel (formerly Altera). We will describe as an example the devices from the 7-Series family produced by Xilinx. These devices include six-input LUTs, integrate up to 120 Mbit of RAM, multi-gigabit transceivers up to 21Gbps, that can be used in main serial communication standards for telecom computing applications (PCIExpress), analog-to-digital converters for measurements of external signals and internal parameters such as chip temperature, voltages applied to the power domains of the device.

Fig.3.1 shows a simplified representation of the configuration memory layout.

For Xilinx device, the floor-plan is divided into two main regions: top and bottom. Each region is organized in rows and columns, the memory of the FPGA

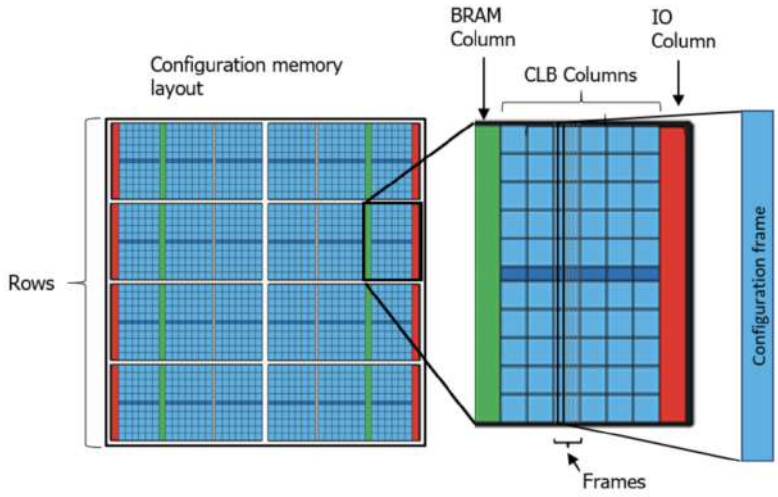

Figure 3.1: Simplified representation of the configuration memory layout is shown [30].

is divided into frames, the set of frames constitutes the configuration of the board, each frame in turn is divided into bits. One frame has the height of a row, and the columns are arranged according to the type of resource (i.e. CLB, BRAM, DSP, etc.). Each column contains a group of frames. The number of frames in each column depends on the type of column as shown in Table 3.1.

Column Type	Number of Frames
CLB	36
DSP	28
Block Ram (configuration)	30
IOB	54
CLK	4

Table 3.1: Number of frame in different columns types in Spartan 7 series. Source [31].

The configuration memory can be accessed from outside or inside the device through several interfaces. Example of external interfaces are: Joint Test Action Group (JTAG), Byte Peripheral Interface (BPI), Serial Peripheral Interface (SPI) and SelectMAP.

The SelectMAP is a proprietary interface that is a programmable parallel interface that can achieve up to 3200 Mbps of data throughput and therefore it provides the fastest configuration time [31]. The ICAP interface, on the other

side, is the internal configuration port of Xilinx FPGAs. It has the same interface as the SelectMAP, but the ICAP can be accessed from the configurable logic [32].

3.1.1 Programmable interconnect

Programmable interconnect is the heart of the FPGA. The logical resources in an FPGA are pre-built on the chip and they are connected in the programming phase. In this layer two elements are distinguished: switch-matrix and lines.

- Switch matrix. The switch matrix represents the junctions at which the various paths arrive. There are two types of switch matrices: crossing switches and separating switches. If the crossing switch at the intersection of a horizontal and a vertical lines is "ON", the two lines are connected. For the separating switch, if it is "OFF" the line is divided into two electrically isolated segments, if it is "ON", the segments are shorted and the line becomes a single electrical line. The crossing switches are represented by solid circuits and the separating by hollow circles. Figure 3.2 shows a switch matrix.

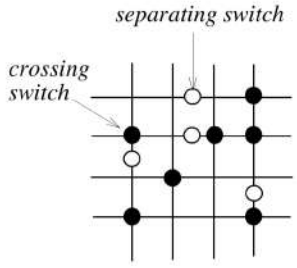

Figure 3.2: Switch matrix.

- Path. The paths (or lines) connect two points in a FPGA. They are divided into long and short, with different properties, and are used for different purposes. Short paths have low propagation delay and lower noise, but cannot connect remote points on the FPGA. Long paths have greater delays,

are less abundant in the device, and inside them newer FPGAs have buffers that act as a repeater.

3.1.2 Programmable logic

In the fabric all the logical resources of the FPGA are instantiated: Configuration logic blocks (CLBs), Input/Output blocks (IOBs), Look-Up Table (LUT), Clock Management Blocks, Block RAM (BRAM), and Digital Signal Processing (DSP) block. Figure 3.3 shows a FPGA architecture representation.

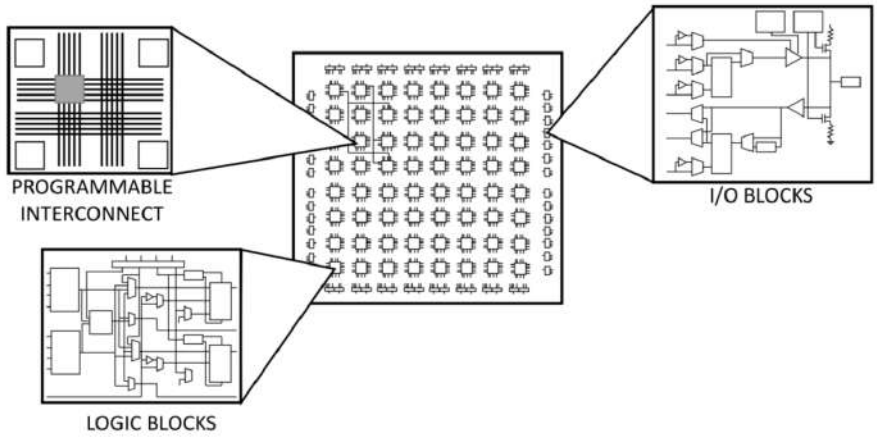

Figure 3.3: FPGA architecture representation.

- A CLB includes two slices and a switch matrix. A slice is composed by LUTs to perform combinational operations, Flip-Flop (FF) as sequential elements, carry chains and multiplexers. LUTs are in modern FPGA devices the basic building block. LUT is an n-bit addressing asynchronous memory. Given a logical function of n variables, the value of the function for any combination of inputs is programmed in the LUT at the address corresponding to the state of the inputs (Fig.3.4). The switch matrix is a system of blocks that are integrated to route signals between multiple inputs and multiple outputs.

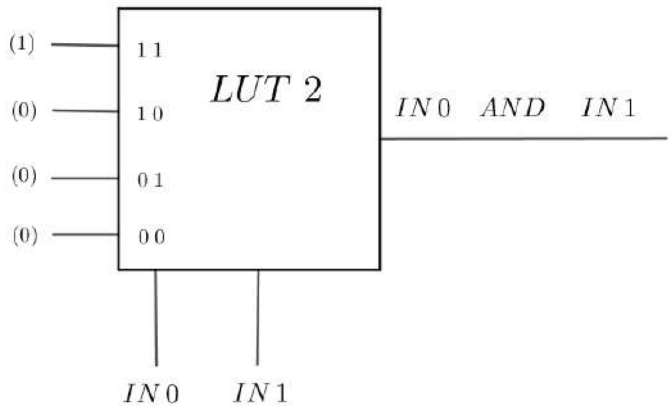

Figure 3.4: Example of how a 2-input LUT works.

This component permits communication between slices in a CLB or between other elements of FPGA and is represented.

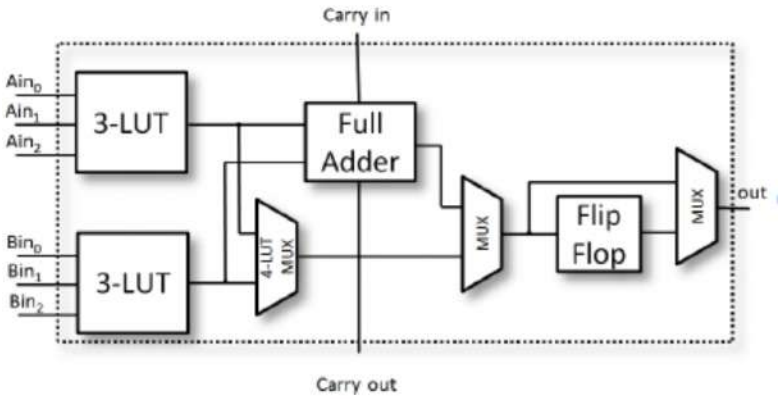

Figure 3.5: Simplified example of an FPGA logic slice.

- IOBs represent the FPGA interface for external connection. These blocks include several components as FFs, resistors, buffers and pads to implement the input and output functions of an FPGA. The FFs are available for data synchronization in order to manage sequential signals. There are buffers to manage different logic standards and to calibrate the input/output current basing on signal fanout. PADs are available to getting data, clocks, power etc, in and out to the FPGA.

- Clock Management Blocks. FPGA has dedicated clock management blocks

allowing to manipulate frequency and phase clock signals and efficiently distribute them in the system.

- BRAM is a dual-port RAM module embedded in the FPGA fabric that provides on-chip storage for a relatively large data sets. Two types of BRAM memories are available in the device: 18k or 36k bits, and the otal number of available memories depends on the device. BRAMs can be configured to be used as smaller blocks if needed. The dual-port nature of these memories makes it possible for parallel, same-clock-cycle access to different locations [33].

- DSP block is an arithmetic logic unit (ALU) embedded in the FPGA fabric and consisting of a chain of three different blocks; among the DSP sub-components, there are an add/subtract unit and a multiplier.

3.2 Soft errors in SRAM-based FPGAs

The errors produced by SEUs in the FPGAs configuration memory can be classified into two different categories: logic and routing errors. Different logic errors may be observed, for example, the SEU can modify one LUT bit, changing the combinational function implemented, or a FF, altering polarity of the reset line or of the clock line. Moreover, a SEU can modify the configuration of a MUX in the logic block, causing wrong signals forwarding inside the logic block. Although a SEU affecting a switch box modifies the configuration of only one PIP, both single and multiple effects can be originated. Single effects happen when the modifications induced by the SEU only alter the affected PIP. In this case one situation may happen, which we call open: the SEU changes the configuration of the affected PIP in such a way that the existing connection between two routing segments is opened.

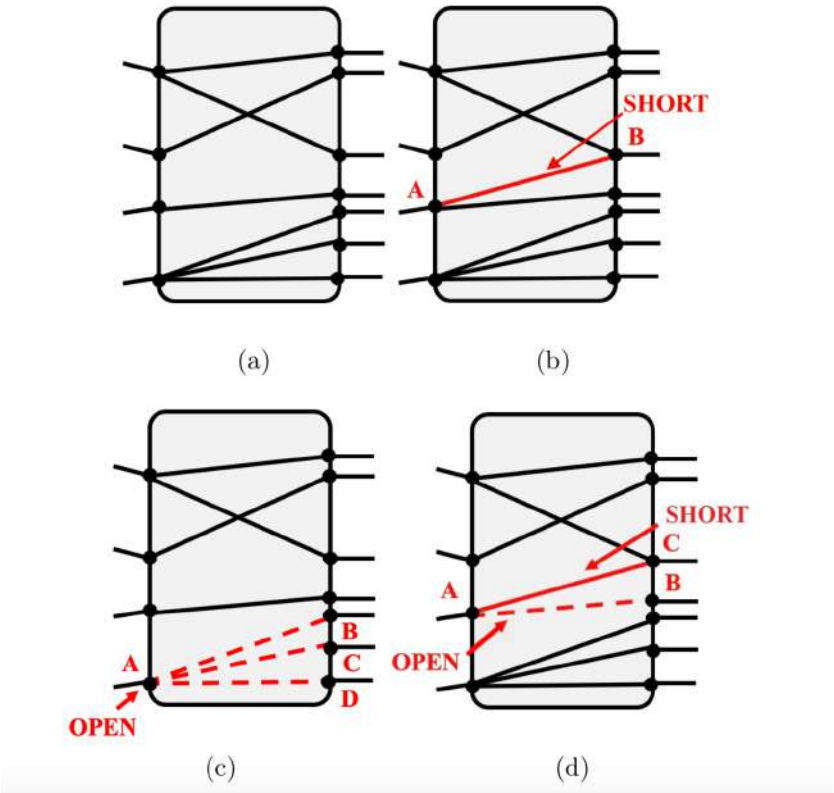

Figure 3.6: Possible multiple effects induced by one SEU: (a) Normal condition, (b) Short effect: creation of a bridge A-B, (c) Open effect: deletion of connections A-B, A-C, A-D (d) Open short effect: interruption of connection between A and B and generation of the A-C bridge.

The multiple effects are described in the following classification.

- Short. SEU modifies he configuration memory bit related on the compound PIP that connects A and B, adding a short between them, as in Fig.3.6(b). This effect can happen when A and B belong to the same switch matrix.
- Open. This situation may happen if a SEU modifies a configuration memory bit belonging to a decoded PIP group and controlling more than one connection (Fig.3.6 (c)).
- Open-Short. This situation may happen if a SEU modifies a configuration memory bit belonging to a decoded PIP a controlling at least connection and deleting a connection (Fig.3.6 (d)).

3.3 Mitigation techniques

As mentioned above, when few devices are needed or for devices that need to change their logic over time, SRAM-based FPGAs provide much higher performance than general-purpose processors for real-time applications. FPGAs also have a lower cost than ASICs. They are reconfigurable, but they are particularly sensitive to radiation-induced SEUs. As a result, the safe use of FPGAs in radiation environments requires careful use of well-proven SEU effects mitigation techniques.

Several methods for enhancing fault-tolerance have been proposed in the past in order to mitigate the effects of SEUs in the configuration memory of FPGAs. These methods could be divided in two complementary categories: redundancy-based methods and configuration-based methods.

Redundancy-based methods aim at masking the propagation of SEU's effects to circuit's outputs and, reconfiguration-based methods aim at restoring, as soon as possible, the proper values into configuration bits after an SEU happened.

The masking does not prevent the accumulation of SEUs,which eventually impair the redundancy scheme. Therefore, redundancy-based methods must be combined with scrubbing to prevent accumulation [34].

We will discuss this issue in more detail in section 3.3.2.

In the following we will describe examples of each the two mitigation technique categories, triple modular redundancy and configuration scrubbing.

3.3.1 Configuration scrubbing

For SRAM-based FPGAs, scrubbing is the collective name given to a range of techniques used to refresh (or re-program) the configuration memory, in some cases by detecting (readback) and correcting (writeback) errors in the background during normal device operation to prevent the accumulation of SEUs.

Regarding the architecture criteria, it is possible to classify scrubbers by the location and the implementation method. The classification is summarized in Fig.3.7. The event that triggers the scrubbing process can classify scrubbers in

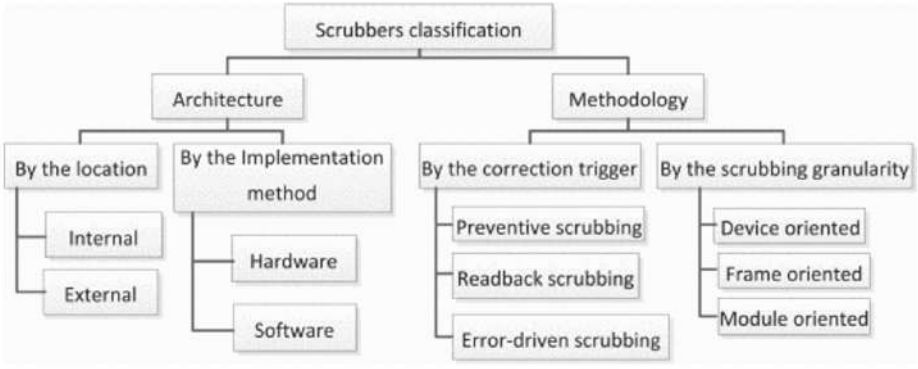

Figure 3.7: Scrubbers classification.

three different methodologies. The first is known as a blind scrubbing. This methodology implements a preventive scrubbing and is the simplest methodology. The scrubbing period can be fixed or adaptive that is, it can occur after a fixed time or after an event that acts as a trigger. On the other hand, readback scrubbing

refers to do periodical readbacks until an SEU is detected; only then a correction is executed. With a readback scrubbing methodology, it is possible to achieve lower energy consumption since only when a soft error is detected, the scrubbing is enabled. Furthermore, this type of scrubbing makes it possible to correct only the affected configuration frames, reducing the configuration repair time. The soft error detection during readback can be implemented using Error Detection and Correction Codes (EDAC) on the configuration frames or by comparing the configuration data with an external reference, usually a radiation-hardened external memory that keeps a copy of the original configuration. The third methodology is the functional error-driven scrubbing. A scrub cycle is enabled when the scrubber receives an error signal from the functional design. This can be used in TMR designs where the voter can detect a module with functional error [36].

The scrubber can be internal or external to the device as schematized in Fig.3.8.

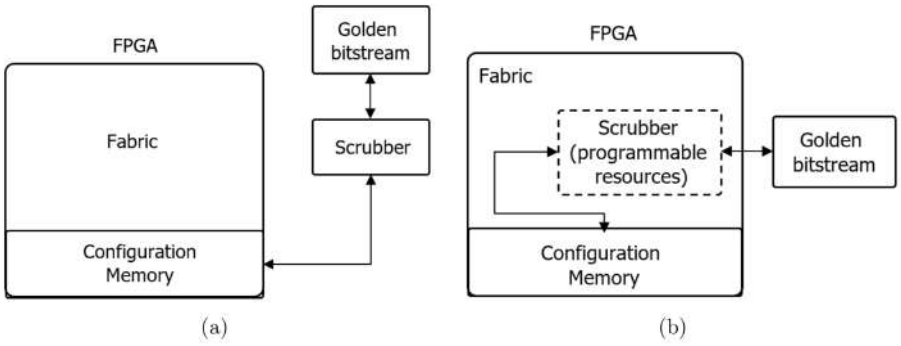

Figure 3.8: Scrubber on FPGA. (a) External implemented scrubber. (b) Internal implemented scrubber.

An internal scrubber makes the system more compact but the scrubber itself can be impacted by SEUs, which can affect also its functionality. As far as the external-scrubber implementation concerned, it is possible to place it in a radiation-free zone in order to safeguard its functionality by avoiding SEUs effects, but this is not always available.

Moreover, internal scrubbing takes less time to work because it does not have

to transport data to the outside. The scrubbing method in the form of partial or full reconfiguration is mandatory for adopting SRAM-based FPGA in the presence of SEUs. Indeed, these techniques are the only viable solution to prevent the accumulation of SEU in the configuration memory, and, therefore, not break redundancy schemes, such as TMR.

3.3.2 Triple Modular Redundancy

Using the redundancy-based techniques to detect the presence of SEUs and/or mask their propagation to the outputs of the circuits, it is necessary to use additional hardware components or increase the processing times.

A widely used method for this aim is the Triple Modular Redundancy (TMR).

The main objective of using a TMR design methodology is to remove all single points of failure from the design. This begins with the FPGA inputs. If a single input was routed to all three redundant logic paths within the FPGA, then a failure at that routing would cause these errors to propagate through all the redundancies, and thus the error would not be masked. Therefore, each redundant logic part of the design that uses FPGA inputs should have its own set of inputs, with independent routing (Fig.3.9). Thus, if one of the input path fails, it will only affect one of the redundant logic blocks. The outputs are the key to the overall TMR strategy. Since the full triple module redundancy triplicates every logic path, the TMR output majority voters, inside the output logic block, allow converging the output again to one signal outside the FPGA, as presented in Fig.3.9.

The probability that an upset in the routing overcomes the TMR is related to the routing density and logic placement. In Fig.3.9, there are two examples of upsets in the routing. Upset “a” connects two signals from the same redundant part, which does not generate an error in the TMR output, because the upset effect will be voted by the outermost voters. However, upset “b” may cause an

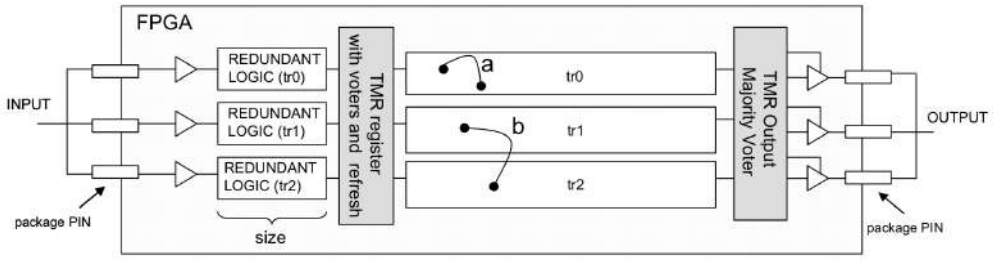

Figure 3.9: TMR Scheme in the FPGA [35].

error in the TMR output, because it connects two signals from distinct redundant logic parts affecting two out of three redundant parts of the TMR.

Dedicated floorplanning for each redundant part of the TMR can reduce the probability of upsets in the routing affecting two or more logic module by placing in distinct areas of the FPGA. However, it may not be sufficient, since placement can be too complex in some cases [35].

Table 3.3 describes SEU effects and consequences in different components of the FPGA.

User Location	Effect	Consequences	Upset correction
LUT	Modification in the Combinational logic	Error in one redundant part with no error in the TMR design output	By scrubbing
Routing	Connection or disconnection between any two or more signals in the design	Error in the redundant part with no error in the TMR design output Error in more than one redundant part with error in the design output	By scrubbing
Customization logic in general	Connection or disconnection between any two in the same CLB	Error in the redundant part with no error in the TMR design output Error in more than one redundant part with error in the design output	By scrubbing
Flip-Flops	Modification in the sequential logic	Error redundant part no error in the TMR design output	By design modification

Table 3.2: Analysis of the possible effects and consequences in TMR design in FPGAs [35].

The reliability $R(t)$ is the probability that a system operates correctly at a time t given that was operating correctly at t=0. Considering a number N of systems, one can define the failure rate $\lambda(t)$, i.e., the number of failed systems ($N_f(t)$) in an infinitesimal time interval dt, normalized with respect to the number of survived systems ($N_s(t)$).

By definition

$$R(t) = \frac{N_s(t)}{N}, \tag{3.1}$$

$$\lambda(t) = \frac{1}{N_s(t)} \frac{dN_f(t)}{dt}. \tag{3.2}$$

Therefore

$$\frac{dR(t)}{dt} = \frac{dN_s(t)}{Ndt} = -\frac{dN_f(t)}{Ndt} = -\frac{1}{N}\frac{dN_f(t)}{dt} = -\frac{\lambda(t)N_s(t)}{N} = -\lambda(t)R(t), \tag{3.3}$$

hence

$$ln\frac{R(t)}{R(0)} = -\int_0^t \lambda(t')dt'. \tag{3.4}$$

Since the system correctly operates at the initial time, i.e., R(t = 0) = 1, the final expression for reliability is

$$R(t) = e^{-\int_0^t \lambda(t')dt'}. \tag{3.5}$$

In a system with a constant failure rate λ(t) = λ, the system reliability $R(t)$ decays exponentially:

$$R(t) = e^{-\lambda t}. \tag{3.6}$$

As the mean time to failure (MTTF) is defined as

$$MTTF = \int_0^\infty R(t)dt, \tag{3.7}$$

then it holds

$$MTTF = \frac{1}{\lambda}, \tag{3.8}$$

For a system with implemented TMR, reliability and MTTF are respectively

$$R_{TMR} = \binom{3}{3}R^3 + \binom{3}{2}R^2(1-R) = 3R^2 - 2R^3 = 3e^{-2\lambda t} - 2e^{-3\lambda t}, \tag{3.9}$$

where $\binom{3}{3}$ is the number of modes in which all modules can be operating correctly and $\binom{3}{2}$ is the number of modes in which one module can fail while the other two are operating correctly.

Consequently

$$MTTF_{TMR} = \frac{3}{2\lambda} - \frac{2}{3\lambda} = \frac{5}{6\lambda} < MTTF. \tag{3.10}$$

Therefore, the mean time to failure in TMR systems is lower than the MTTF of the single modules, as shown in Fig.3.10.

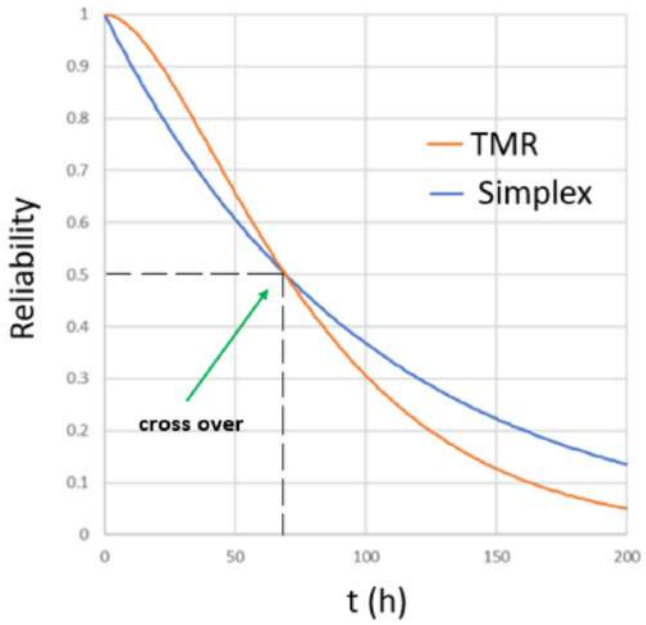

Figure 3.10: Reliability in function of time for a single system and a TMR system. MTTF = $100h$ and the cross over occur

In order to have a beneficial impact of the TMR on reliability, $R(t)$ must be larger than 0.5, so we introduce a correction mechanism (i.e. the scrubbing) which restores $R(t)$ to higher values periodically by removing configuration upsets.

3.3.3 Redundant-Configuration-based Scrubbing

Typically the current state of the art provides that there are three FPGAs, which are configured in the same way, and an external scrubber. Even if this leads to a solution to the problem, it is not always suitable, as: there is an increase in set up costs, necessary space, consumption and weight of the setup.

A preferred solution is to redundant configuration on a single board, keeping only one copy working and the other two will be exploited by a scrubber as a gold configuration. The other two copies can be divided into modules and divided into different parts of the FPGA.

This type of solution has been patented [39] and has proved to be valid for many FPGAs of the Xilinx family. The method of this patent is a protection mechanism for the configuration but not for the logic.

As described so far, this approach does not require external memories to store the configuration and therefore, also maintaining the internal scrubber, the FPGA does not need communicate with the outside so the downtime of the device decreases. If the SEU impacts the scrubber functionality, it will be necessary to re-enter the configuration from the outside.

A scrubber of this type can be adaptive and in this case there is the advantage that it decreases the number of resets that the device has to perform. In the next chapter the two types of scrubbers, external and internal, will be examined in more detail.

3.3.4 Configuration Consistency Corrector Architecture

In [30] the authors designed the Configuration Consistency Corrector (C^3) scrubber, implemented as a triple modular system. Fig.3.11 shows a simplified block diagram of C^3.

Before operating, the C^3 requires some preliminary operations to be performed

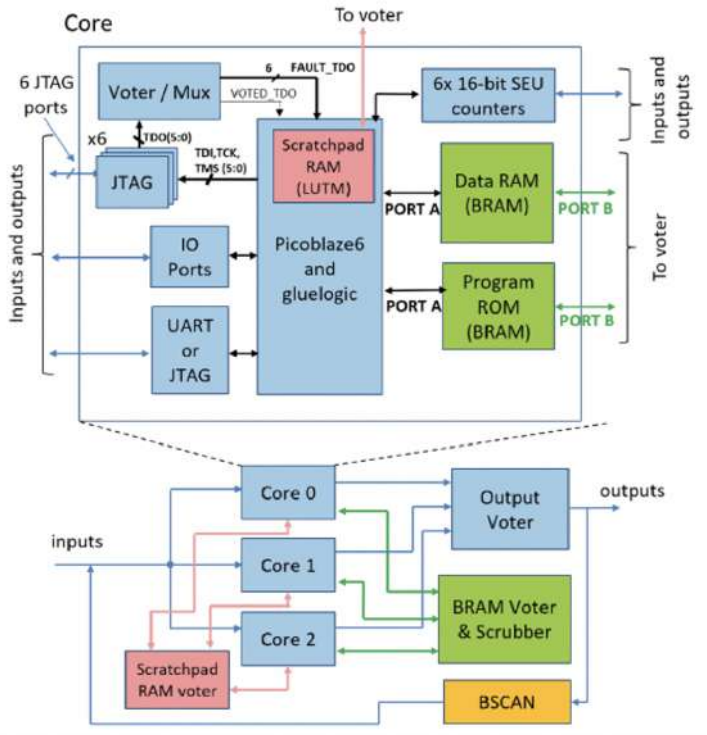

Figure 3.11: Simplified block diagram of C^3. Bottom: overall architecture with cores in TMR scheme. Top: close-up on a core [30].

on the configuration. These operations include the identification of used and non-used configuration frames in order to perform the redundancy of the configuration through the following steps:

1. The identification of used and non-used configuration frames;
2. The replication of configured frames to obtain three redundant configuration copies;
3. The identification of the remaining empty frames.

During the FPGA operation, the C^3 performs a continuous majority voting of replicated frames for error detection and correction. Moreover, empty frames are checked to remain in their default status (all bits are zero) and if not they are forced to it.

The realized scrubber is implemented in software running on picoBlaze (pB),

which is a lightweight 8-bit soft microcontroller provided by Xilinx and supported by most device families.

The C^3 architecture consists of three cores (Core0, Core1, and Core2), which in turn include the mentioned pB, a 4k by 18-bit words (Program ROM), a 4k by 8-bit words memories (Data RAM), and glue logic for IO port.

Other core components are the Data RAM and Program ROM scrubbers, which manage the rewriting of BRAMs contents when a mismatch in one of the cores memories is found. Regarding the configuration scrubbing, it is performed through majority voters mechanism as well and by preserving the state of the unprogrammed frames. As previously mentioned, the access to the configuration is performed via ICAP, that cannot be tripled due to the FPGA structure.

Therefore, a dedicated majority voter for the cores signals destined to the ICAP has been designed, in order to preserve the operation to the FPGA configuration. Furthermore, the C^3 uses the JTAG port for I/O communication and employs the JTAG Loader resource to update the Program ROM at run time. Finally, the DCO generates the clock signal to distribute within the self-repair circuit and there is a counter, named Unixtime counter, which is clocked on the DCO [**?**].

In the next chapter we will introduce the core of this thesis: an automatic tool to generate a triple configuration for FPGAs. The tool automates the process related to the above-mentioned steps 1-3.

Chapter 4

Automatic Generation of Redundant Configuration

In this chapter we introduce a software tool which realizes configuration redundancy by copying the programmed frames content into unused ones.

4.1 Idea

The tool that we present, and that we call Redundant Configuration Generator (ReGen), is based on the [39] patent which involves the use of a single board and internal scrubber. The use of the protocol described by the patent leads to the decrease of resources used and the current consumption and the operating frequency of the design does not vary from that without triplicating.

It provides configuration but not logic protection and requires a dedicated configuration which l can also be generated manually, but this is a time consuming task, since each time a small modification is made to the design, the generation of the redundant configuration must be performed again.

The tool should be seen as an extension of the project flow (Fig.4.1) that leads to the generation of the FPGA configuration. To do this we had to write libraries

for communicating with the board and scripts. The programming language we have chosen is TCL, as TCL can be integrated with the Xilinx development tool (VIVADO)

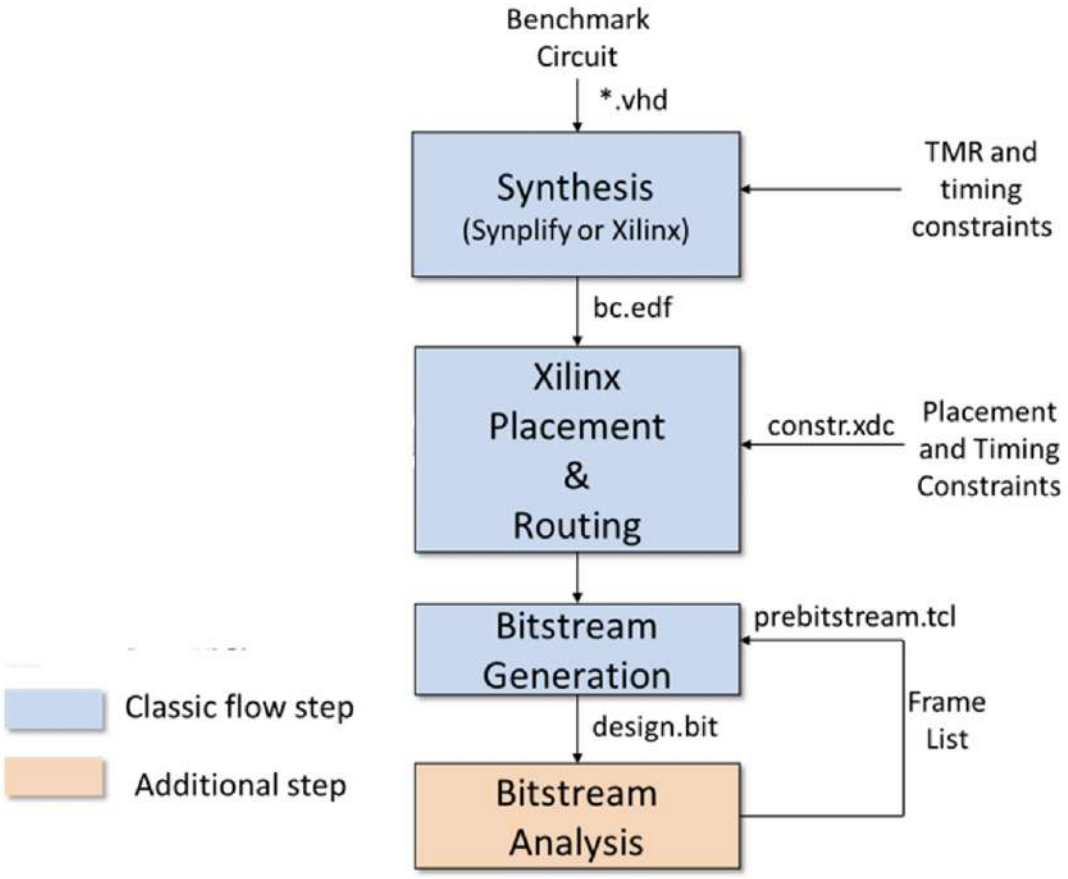

Figure 4.1: Design Flow with TMR.

The basic idea of the ReGen method is:

1) consider the configuration as a set of frames without being interested in the type of logical resource that they will configure;

2) copy the contents of the programmed frames into unprogrammed areas of the FPGA;

3) insert in the BRAMs the information that allows the C^3(or any dedicated scrubber) to identify where the blocks of programmed frames and their copies

are.

To do this we divide the initial configuration into blocks (Fig.4.2), a subdivision which can follow various criteria which we will discuss later. Subsequently we carry

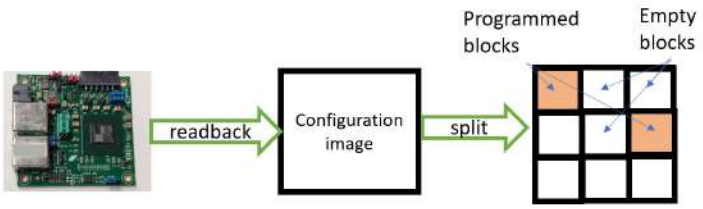

Figure 4.2: Configuration block classification.

out an analysis on the blocks to separate the programmed ones and the empty ones. Therefore, for each programmed block, two possible destinations are sought in the list of empty blocks (Fig.4.3).

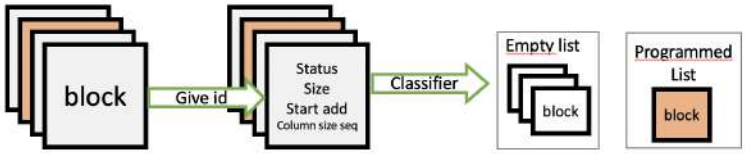

Figure 4.3: Have to separate programmed blocks from empty ones.

Once these are found, they will be tested by analyzing the current consumption (Fig.4.4). Sometimes it is not possible to find a solution for an entire block so

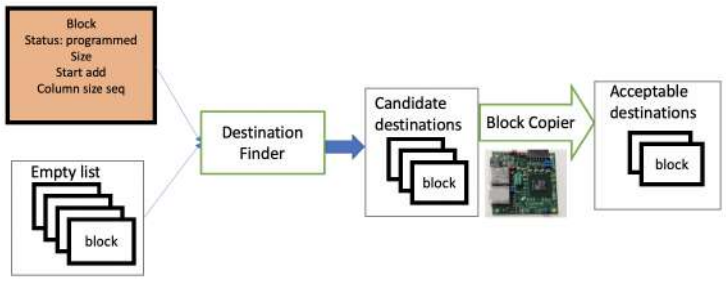

Figure 4.4: Testing of the possible destinations.

ReGen re-sizes it and try to find destinations for the generated sub-blocks. The splitting of the blocks that ReGen do must keep the number of blocks as low as possible, this serves to make the scrubber faster and to decrease the amount of BRAM needed.

4.2 Hardware setup

The hardware setup includes a controller personal computer, a custom FPGA-based board and a power analyzer (Keysight N6705C) (Fig.4.5).

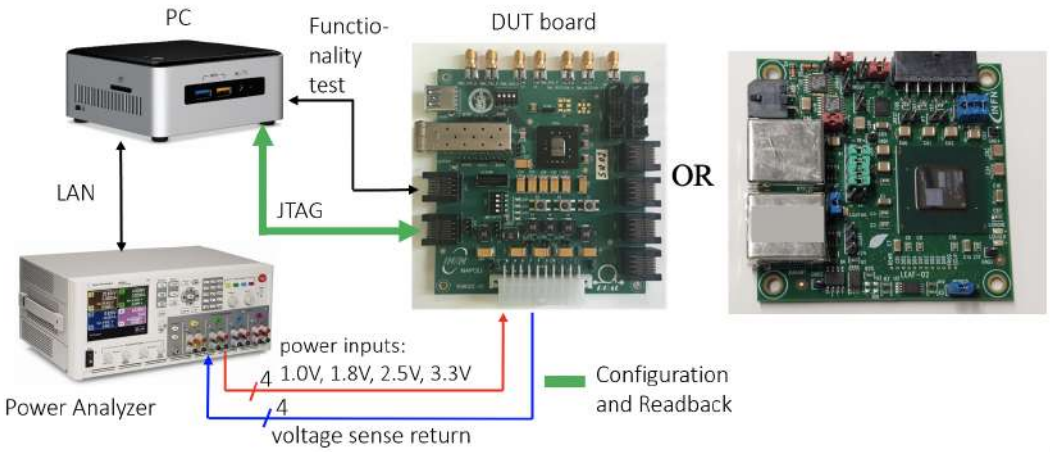

Figure 4.5: Simplified block diagram of the hardware setup.

The PC is interfaced to the target FPGA via a JTAG interface for configuration IO and to the power analyzer via an ethernet connection.

Communication via JTAG is also managed by a custom Ethernet-board called branch (Fig.4.6), which in turn communicates with the computer with another board designed by INFN Napoli called cora (Fig.4.7).

PC runs ReGen, it processes all the information that is collected and selects which destinations to test and whether they comply with the constraints. It is the means used by the user to interface with the setup.

The FPGA is needed to measure power consumption but also readback and functional testing.Moreover, in FPGAs there are some frames where it is not

Figure 4.6: Branch.

Figure 4.7: Cora Z7, interface board.

possible to write a configuration. The presence of the board in this set up is also necessary to identify its blind spots. In principle it would be possible to enter this information from the outside, at the beginning or at a later time, but doing so the script would lose generality. As this file should be updated every time a new FPGA family comes out.

The power analyzer supplies current and provides information on the consumption by the FPGA. The number of power analyzer channels required varies from board to board. As regards the currents, however, if the tripling is carried out effectively only the core current will show variation.

4.3 Implementation

ReGen follows the flowchart described in Fig.4.8 starts with FPGA readback.

The PC communicates via JTAG black with the FPGA (using another custom board). A file describing the configuration is thus generated which will then be inserted into the ring structure described in the Fig.4.9, within which it is updated. This process is to avoid having to re-read the FPGA every time we write something on it. In this way this action, which is the most time-consuming of the whole process, is only carried out at the beginning. Frames are extracted from the configuration file obtained after the first reading, which in turn are grouped into blocks. The blocks undergo a first classification that distinguishes them from programmed and empty.

In this phase we also give attributes: size of the block, column size sequence and first minor address to the various blocks that will be used to find compatible destinations for the various programmed blocks.

This first skimming is essential because by doing so you avoid going to make a totally blind copy. Also, since the FPGA configuration drive also routing resources which can be driven with apposite logical values and levels, this selection avoids a

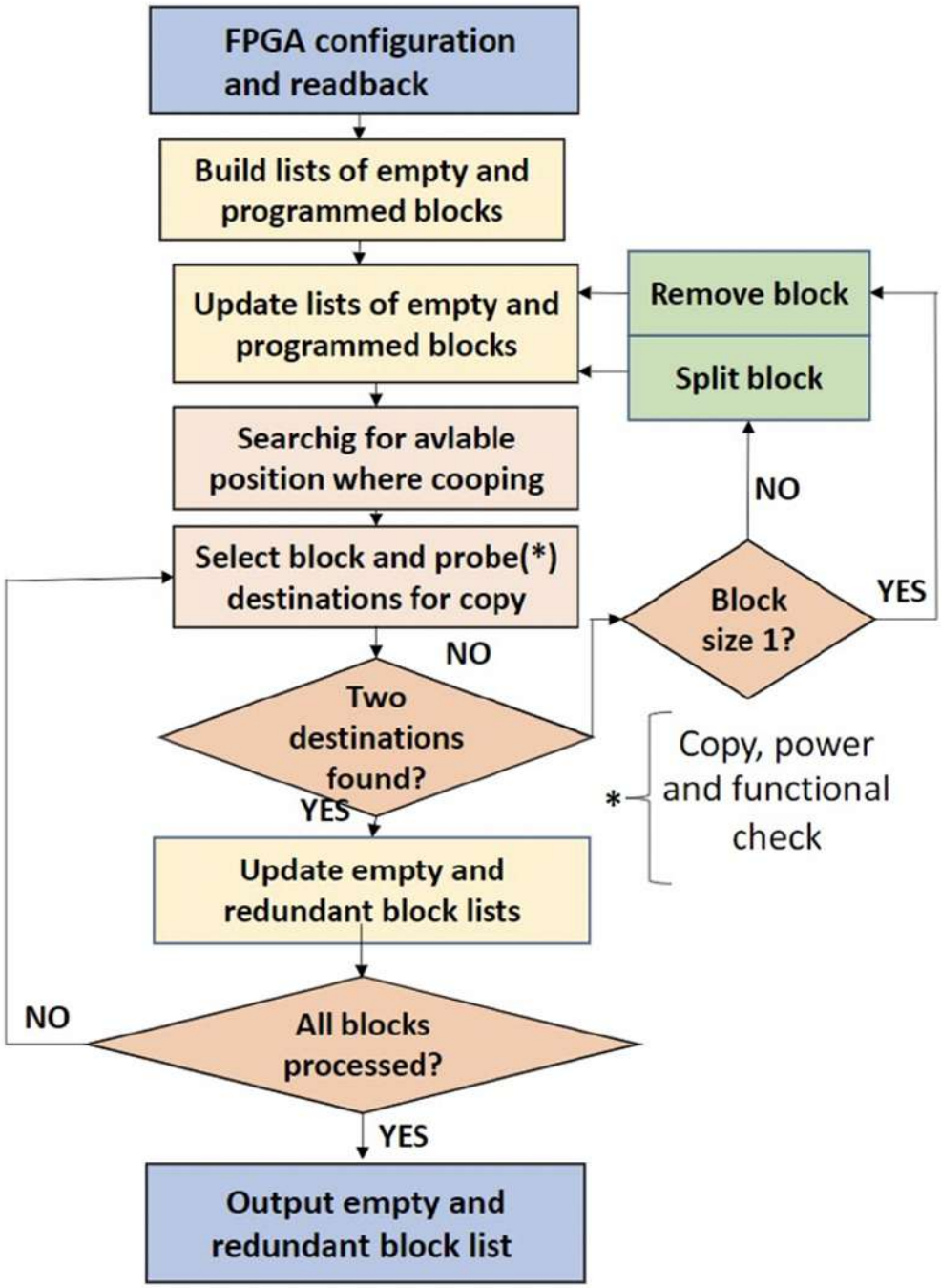

Figure 4.8: Flow-chart.

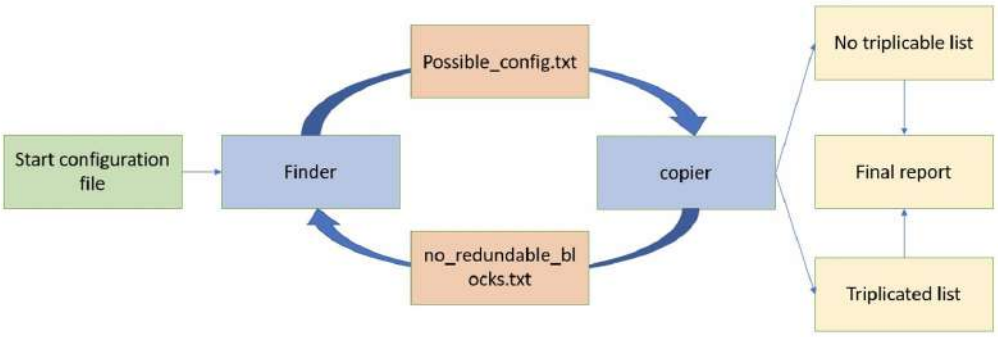

Figure 4.9: Redundant configuration generation flow.

configuration that can break the device. Another advantage that is obtained from this pre-processing is that by eliminating some possible destination immediately, the test process of the possible destination is considerably accelerated.

The file generated by the process described above is used by another script (copier) that tests the various solutions and analyzes the absorbed currents. It is also an access point for the user who can modify it with the help of external programs to impose constraints on the blocks to be triplicated and on the destinations. It will copy all the blocks in order to first process those with the least possible destination, then it will test the blocks in the various destination found and, if it is possible, it copies in whole blocks, otherwise it works with partial solutions splitting the blocks in smaller ones.

Once the frames to be redundant have been written in the positions indicated by finder, the current is analyzed and if the testis passed , copier updates the configuration file, otherwise it returns the configuration to the state prior to the attempt made. If copier does not find any partial solution, the first frame of the block is classified as not triplicable while the remaining portion of the block is inserted in a file that is sent to finder which will repeat the cycle. It is also possible to send non-triplicable frames back to finder, thus being able to set adaptive constraints on the number of cycles that this ring structure has performed.

The blocks for which two compatible destinations were found are added with this information to a report file, from which constraints will be generated that will indicate the content of the BRAMs. This allows the scrubber to work.

4.4 Test results

We tested ReGen on selected firmwares on two FPGA-based boards, a first one based on a Kintex-7 70T and a second one based on an Artix-7 200T.

The 4 designs we analyzed implemented a configuration scrubber, they were chosen because we already had redundant configurations done manually of the latter. They had very different resource occupation characteristics as we can see in the synthesized design in Fig.4.10 and in Fig.4.11. Both designs feature scrubbers leaf_dco for Artix-7 200T and scrubber_dco for Kintex-7 70T.

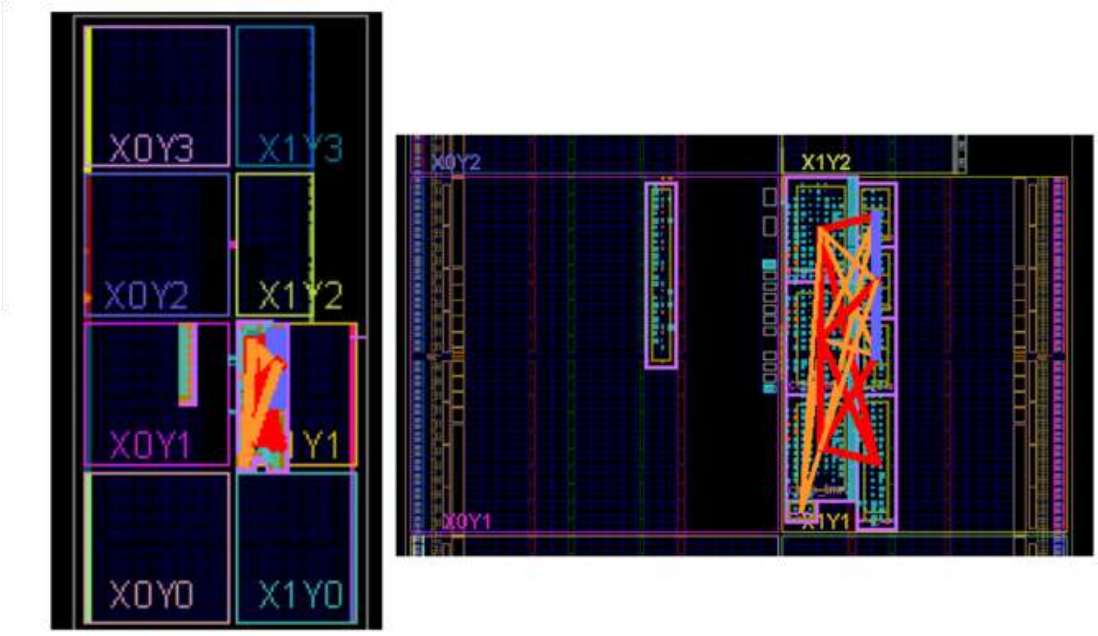

Figure 4.10: Placement of a tested design on Artix-7 200T.

We made our tool work on projects that had already been done triplication manually and then we compared the results obtained to verify its effectiveness, as

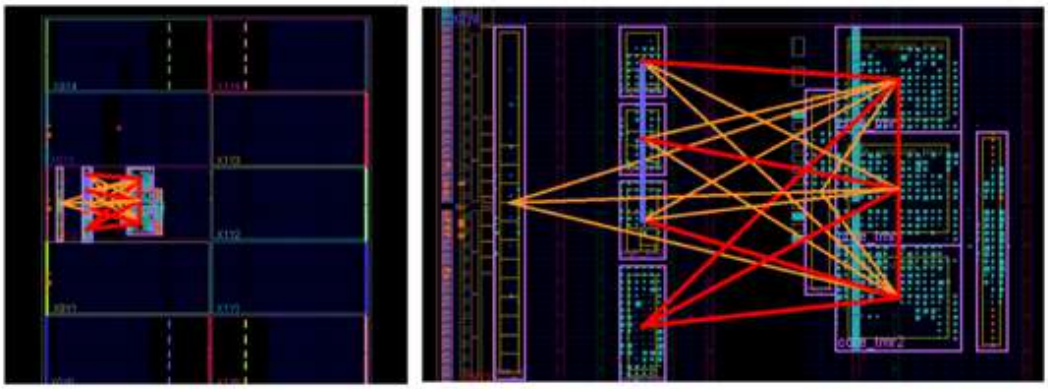

Figure 4.11: Placement of a tested design on Kintex-7 70T.

for the execution time, the tool is not only much faster provided a configuration that triples more completely than what was done manually. The total dissipated current is practically the same, in fact already manually the increase in current is equal to 0.

Among the various projects we worked on, I focused on a configuration scrubber called leaf_dco which runs on Artix-7 200T board.

Fig.4.12 shows the logical resources used by Vivado tool to synthesize this design.

Our tool was able to triple 99.5% of the entire configuration We now show the current data regarding leaf dco. In Fig.4.13, Fig.4.14 and Fig.4.15 four operating phases can be distinguished for the 3 channels.

At first the board is switched off and not programmed, then it is programmed and switched on, then there is the phase in which triplication takes place and finally the current absorbed is shown when the board is in operation and programmed with a redundant configuration.

Highlighting more only the time period during which our script worked graphs are obtained the following grafics Fig.4.16, Fig.4.17 and Fig.4.18.

Note that tripling only significantly impacted only one channel of the power analyzer (Fig.4.16).

Name	Slice LUTs (133800)	Block RAM Tile (365)	Bonded IOB (285)	ILOGIC (285)	OLOGIC (285)	BUFGCTRL (32)	BUFHCE (120)	BSCANE2 (4)	ICAPE2 (2)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)
ccube_leaf	2174	9	23	3	9	4	1	1	1	1813	66	24	823	1958	216
dco_clk.GiordanoDCO_inst (GiordanoDCO)	188	0	0	0	0	0	1	0	0		0	0	109	188	0
inst_scrubber (scrubber)	1976	9	0	0	0	1	0	1	1		66	24	711	1760	216
minvot_tck (minority_voter)	2	0	0	0	0	0	0	0	0		0	0	1	2	0
minvot_tdi (minority_voter_0)	2	0	0	0	0	0	0	0	0		0	0	1	2	0
minvot_tms (minority_voter_1)	2	0	0	0	0	0	0	0	0		0	0	1	2	0
minvot_uart_tx (minority_voter_2)	2	0	0	0	0	0	0	0	0		0	0	2	2	0
minvot_user_led (minority_voter_3)	2	0	0	0	0	0	0	0	0		0	0	2	2	0

Figure 4.12: Resources occupation of a tested design on Artix-7 200T.

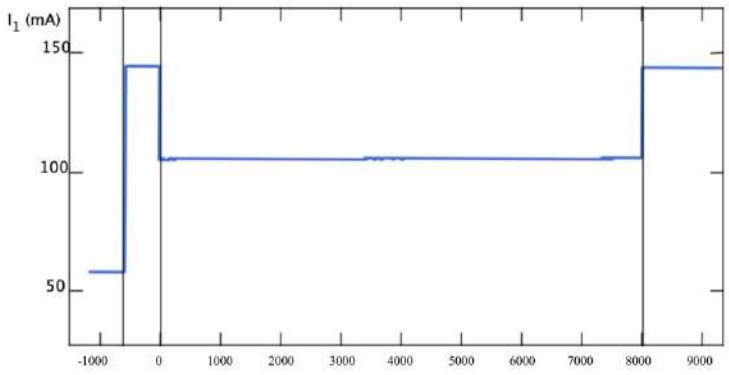

Figure 4.13: Current in mA vs frames triplicated in first channel during all the process.

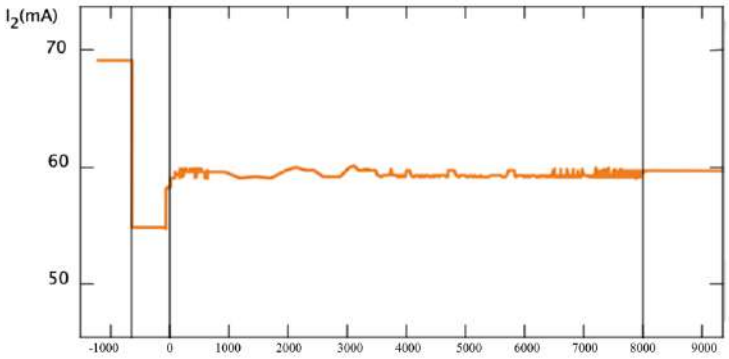

Figure 4.14: Current in mA vs frames triplicated in second channel during all the process.

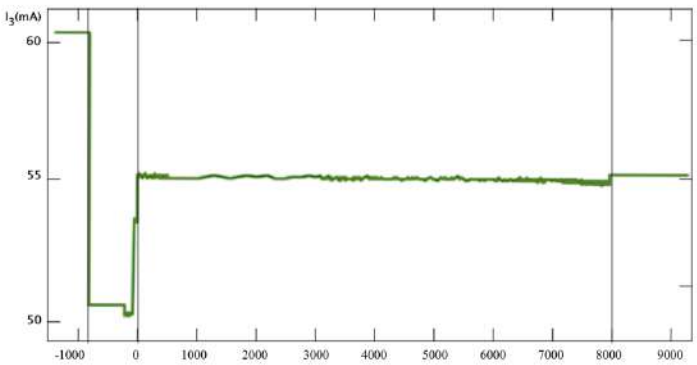

Figure 4.15: Current in mA vs frames triplicated in third channel during all the process.

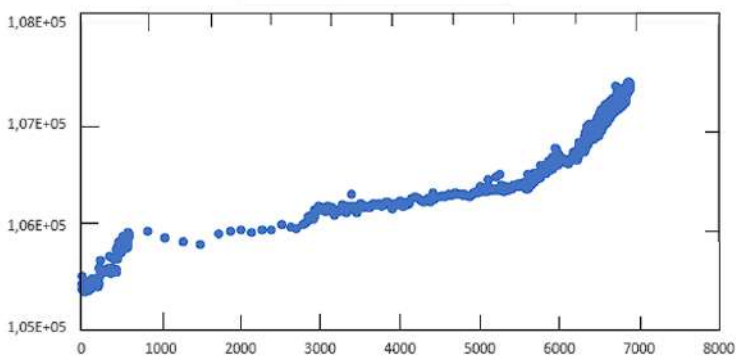

Figure 4.16: Current in μA vs frames triplicated in first channel during copier.

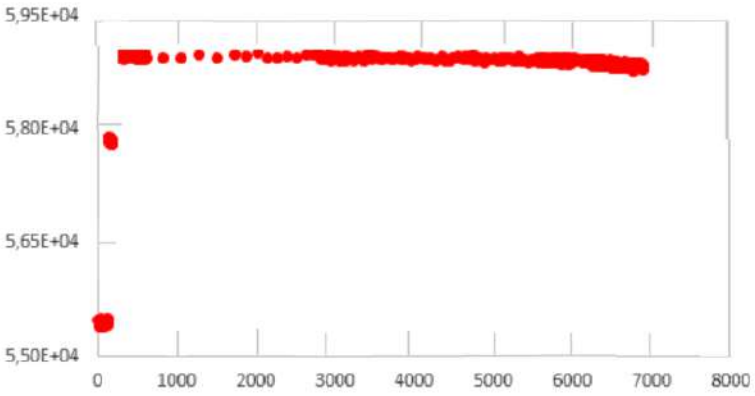

Figure 4.17: Current in μA vs frames triplicated in second channel during copier.

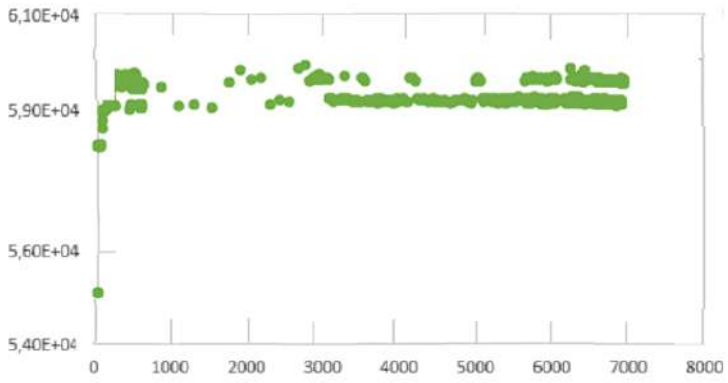

Figure 4.18: Current in μA vs frames triplicated in third channel during copier.

Once the triplication has been performed, our test concludes with a functional analysis. During triplication, spikes in current consumption can be seen, this effect is what we used to understand whether or not the copy destination was compatible with resource.

For future projects, the goal is to include this functional test within the triplication itself. The times required for tripling are therefore significantly lower we expected, going from several hours of manual triplications to a few minutes.

Conclusion

I have developed a software tool to automate a patented method to generate a redundant configuration memory content in an FPGA. The tool does not depend on internal details of the FPGA device. It can potentially used with any FPGA, the only requirement being that the device has a bidirectional configuration access port, i.e., allowing programming and readback. Differently from other tools in the literature, it is based on actual measurements on the hardware (compatibility of frames for copying, test, power consumption).

The work of the thesis has been carried out in the framework of the PHI experiment. The aim of the experiment is to design hadron fluence sensors built around SRAM based FPGAs.

Test results on selected firmwares and devices are promising and they proved it is possible to generate fully-redundant configurations for device occupations up to 20% with a negligible impact on power consumption. My software tool generates a redundant configuration in a few minutes, while a manual implementation of the patented method would require several hours. Moreover, it performs a more complete configuration, triplicating 99.5% of the configuration, instead manual implementations of the patented method were shown to reach about 98%.

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